phyFLEX®-i.MX 6

Hardware Manual

Document No.: **L-773e_2**

SOM Prod. No.: **PFL-A-XL1-xxx**
SOM PCB. No.: **1362.1**

CB Prod. No.: **PBA-B-01**
CB PCB. No.: **1364.2, 1364.3**

Edition: March 2013

A product of a PHYTEC Technology Holding company

Copyrighted products are not explicitly indicated in this manual. The absence of the trademark (™, or ®) and copyright (©) symbols does not imply that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual.

The information in this document has been carefully checked and is considered to be entirely reliable. However, PHYTEC Messtechnik GmbH assumes no responsibility for any inaccuracies. PHYTEC Messtechnik GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product. PHYTEC Messtechnik GmbH reserves the right to alter the information contained herein without prior notification and accepts no responsibility for any damages that might result.

Additionally, PHYTEC Messtechnik GmbH offers no guarantee nor accepts any liability for damages arising from the improper usage or improper installation of the hardware or software. PHYTEC Messtechnik GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

	EUROPE	NORTH AMERICA
Address:	PHYTEC Messtechnik GmbH Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (6131) 9221-32 sales@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de http://www.phytec.eu	http://www.phytec.com

2nd Edition March 2013

List of Figures

List of Tables

Conventions, Abbreviations and Acronyms

This hardware manual describes the PFL-A-XL1 System on Module in the following referred to as phyFLEX®-i.MX 6. The manual specifies the phyFLEX®-i.MX 6's design and function. Precise specifications for the Freescale Semiconductor i.MX 6 micro-controllers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Note: We refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products. Please read the paragraph "**Product Change Management and information in this manual on parts populated on the SOM**" within the *Preface*.

Note: The BSP delivered with the phyFLEX®-i.MX 6 usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the *i.MX 6 Reference Manual*, if such information is needed to connect customer designed applications.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device

- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyFLEX-Connector always refer to the high density samtec connector on the undersides of the phyFLEX-i.MX 6 System on Module.

Types of Signals

Different types of signals are brought out at the phyFLEX-Connector. The following table lists the abbreviations used to specify the type of a signal.

Signal Type	Description	Abbr.
Power	Supply voltage input	PWR_I
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
IPU	Digital input with pull-up, must only be connected to GND. (jumper or open-collector output)	IPU
OC-Bidir PU	Open collector input/output with pull up	OC-BI
OC-Output	Open collector output without pull up, requires an external pull up	OC
5V Input PD	5 V tolerant input with pull down	5V_PD
LVDS Input	Differential line pairs 100 Ohm LVDS level input	LVDS_I
LVDS Output	Differential line pairs 100 Ohm LVDS level output	LVDS_O
LVDS IO	Differential line pairs 100 Ohm LVDS level bidirectional input/output	LVDS_I/O
TMDS Output	Differential line pairs 100 Ohm TMDS level output	TMDS_O
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O

ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level onput	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 100 Ohm PCIe level input	PCIe_I
PCIe Output	Differential line pairs 100 Ohm PCIe level output	PCIe_O
MLB Output	Differential line pairs 100 Ohm Media local bus output	MLB_O
MLB IO	Differential line pairs 100 Ohm Media local bus bidirectional input/output	MLB_I/O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI-2_I

Table 1: Signal Types used in this Manual

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the phyFLEX Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
GPI	General purpose input.
GPIO	General purpose input and output.
GPO	General purpose output.

IRAM	Internal RAM; the internal static RAM on the Freescale Semiconductor i.MX 6 microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Extension Board
PMIC	Power management IC
PoE	Power over Ethernet
POR	Power-on reset
RTC	Real-time clock.
SMT	Surface mount technology.
SOM	System on Module; used in reference to the PFL-A-XL1 /phyFLEX®-i.MX 6 module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board.

Table 2: Abbreviations and Acronyms used in this Manual

Preface

As a member of PHYTEC's new phyFLEX® product family the phyFLEX-i.MX 6 is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyFLEX® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyFLEX® module lies in its layout and test.

PHYTEC's new phyFLEX® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes while using the newly developed phyFLEX® embedded bus standard. The standardized connector footprint and pin assignment of the phyFLEX® bus makes this new SOM generation extremely scalable and flexible. This also allows to use the same carrier board to create different applications depending on the required processing power. With this new SOM concept it is possible to design entire embedded product families around vastly different processor performances while optimizing overall system cost. In addition, future advances in processor technology are already considered with this new embedded bus standard making product upgrades very easy. Another major advantage is the forgone risk of potential system hardware redesign steps caused by processor or other critical component discontinuation. Just use one of PHYTEC's other phyFLEX® SOMs thereby ensuring an extended product life cycle of your embedded application.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html
or www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyFLEX has the following structure:

PFL-*A*-*xx*-*xxxxxx*.*A2*

Generation

A = First Generation
B = Second Generation

Product number (consecutive)

Assembly options (depending on model)

Version number

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phyFLEX-i.MX6.html or
http://www.phytec.eu/europe/support/faq/faq-phyFLEX-i.MX6.html

Declaration of Electro Magnetic Conformity of the PHYTEC phyFLEX®-i.MX 6

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM

When buying a PHYTEC SOM, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating longlivety of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Change management in case of functional changes

- Avoid impacts on Product functionality by choosing equivalent replacement parts.
- Avoid impacts on Product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our Products.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team for through the given contact information within this manual.

1 Introduction

The phyFLEX-i.MX 6 belongs to PHYTEC's phyFLEX System on Module family. The phyFLEX SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyFLEX boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

PHYTEC's phyFLEX family introduces the newly developed phyFLEX embedded bus standard. Apart from processor performance, a large number of embedded solutions require a corresponding number of standard interfaces. Among these process interfaces are for example Ethernet, USB, UART, SPI, I^2C, PCIe, audio, and display connectivity. The phyFLEX bus exactly meets this requirement with the phyFLEX-fix connector. As well the location of the commonly used interfaces as the mechanical specifications are clearly defined. Beside this, the phyFLEX concept also considers, that different controllers have many different interfaces. To take this into account, the phyFLEX concept allows two more connectors: the phyFLEX-optional connector, which has optional, but defined interfaces at fixed positions (e.g. SATA, CAN, camera) and the phyFLEX-flex connector, which has only fixed Ground signals. All other signals of the phyFLEX-flex connector are module specific. All interface signals of PHYTEC's new phyFLEX bus are available on up to three, high-density pitch (0.5 mm) connectors, allowing the phyFLEXs to be plugged like a "big chip" into a target application.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments approximately 20 % of all pin header connectors on the phyFLEX bus are dedicated to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyFLEX boards even in high noise environments.

phyFLEX boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyFLEX users with access to this cutting edge miniaturization technology for integration into their own design.

The phyFLEX-i.MX 6 is a subminiature (60 mm x 70 mm) insert-ready System on Module populated with the Freescale Semiconductor i.MX 6 microcontroller. Its universal design enables its insertion in a wide range of embedded applications.

Precise specifications for the controller populating the board can be found in the applicable controller reference manual or datasheet. The descriptions in this manual are based on the Freescale Semiconductor i.MX 6. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyFLEX-i.MX 6.

The phyFLEX-i.MX 6 offers the following features:

- Subminiature System on Module (60 mm x 70 mm) achieved through modern SMD technology
- Populated with the Freescale Semiconductor i.MX 6 microcontroller (BGA624 packaging)
- Max. 1.2 GHz core clock frequency
- Boot from different memory devices (NAND Flash (standard))
- phyFLEX bus. Commonly used interfaces such as Ethernet, USB, UART, SPI, I^2C, audio, PCIe, SATA, CAN, display and camera connectivity (both LVDS) are available at up to three high-density (0.5 mm) samtec connector, enabling the phyFLEX-i.MX 6 to be plugged like a "big chip" into target application
- Single supply voltage of 5 V
- All controller required supplies generated on board
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- 1 GB (up to 4 GB) DDR3 SDRAM
- 1 GB (up to 16 GB) on-board NAND Flash

- Up to 16 MB on-board serial Flash (bootable)
- Up to 4 kB I^2C EEPROM
- Serial interface with 4 lines (TTL) allowing simple hardware handshake
- High-Speed USB OTG transceiver
- High-Speed USB HOST transceiver
- 10/100/1000 Mbit Ethernet interface
- Two I^2C interfaces
- Two SPI interfaces
- PCIe Interface
- I^2S Interface
- CAN interface
- Media Local Bus (MLB) interface
- 4 Channel LVDS (24 Bit) LCD-Interface
- HDMI interface
- Two LVDS Camera Interface
- Two SD/MMC card interfaces
- SATA interface
- Support of standard 20 pin debug interface through JTAG connector
- Eleven GPIO/IRQ ports (with phyFLEX-flex connector even more)
- Two user programmable LEDs
- Power Management IC (PMIC)
- Optional Environment Management IC (EMIC) to monitor voltage, current and temperature, and for fan control
- One Wake Up input
- Industrial temperature range (-40 °C to +85 °C)

1.1 Block Diagram

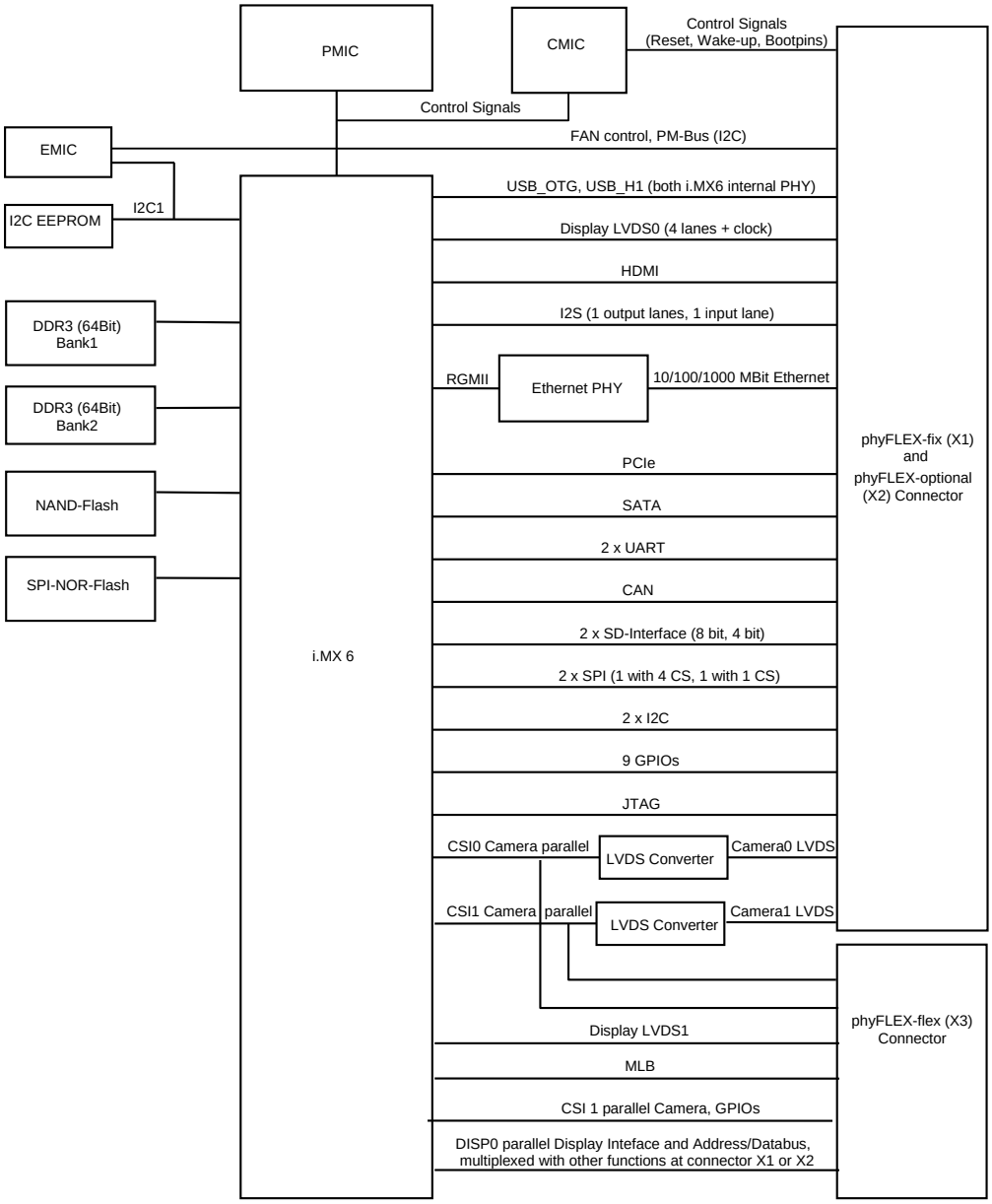

Figure 1: Block Diagram of the phyFLEX-i.MX 6

1.2 phyFLEX-i.MX 6 Component Placement

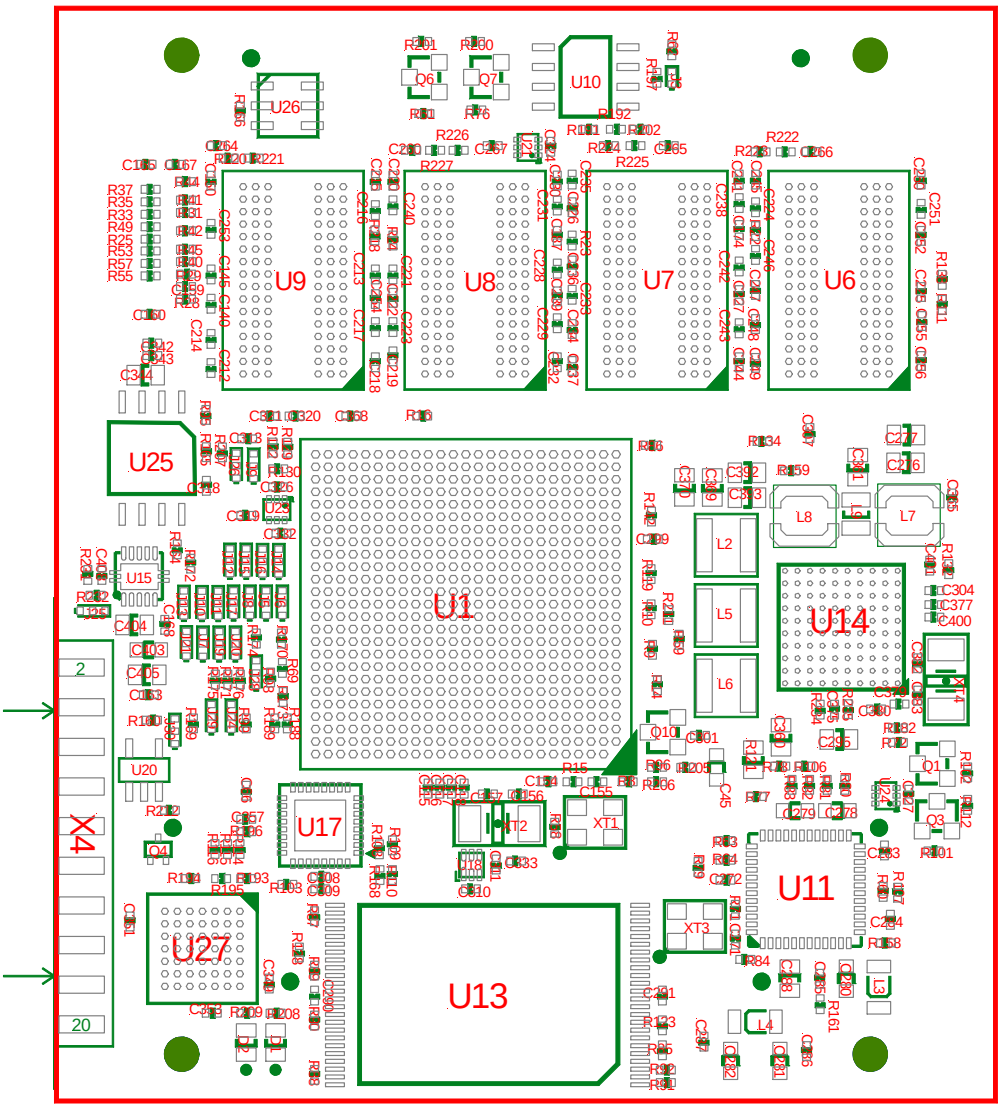

Figure 2: phyFLEX-i.MX 6 Component Placement (top view)

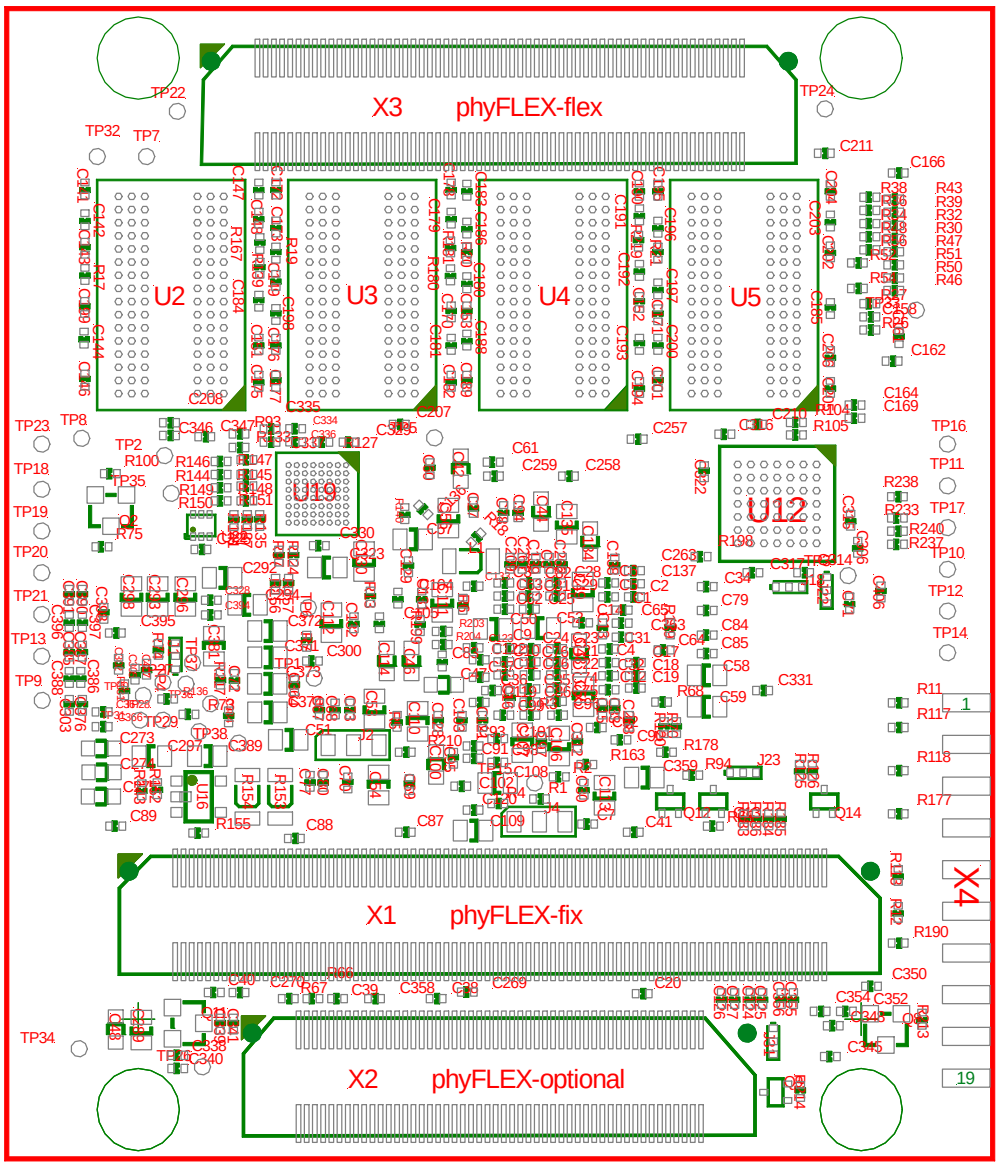

Figure 3: phyFLEX-i.MX 6 Component Placement (bottom view)

1.3 Minimum Requirements to operate the phyFLEX-i.MX 6

Basic operation of the phyFLEX-i.MX 6 only requires supply of a +5 V input voltage with 2 A load and the corresponding GND connection.

These supply pins are located at the phyFLEX-Connector X1:

VDD_5V_IN_R: X1 A1, A2, A3, B1, B2, B3

Connect all +5 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 A4, A10, A16, B4, B7, B13

Please refer to *section 2* for information on additional GND Pins located at the phyFLEX-Connector X1.

Caution:
We recommend connecting all available +5 V input pins to the power supply system on a custom carrier board housing the phyFLEX-i.MX 6 and at least the matching number of GND pins neighboring the +5 V pins.

In addition, proper implementation of the phyFLEX-i.MX 6 module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to *section 4* for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all phyFLEX bus signals extend to up to three surface mount technology (SMT) connectors (0.5 mm) (referred to as phyFLEX-Connector). This allows the phyFLEX-i.MX 6 to be plugged into any target application like a "big chip". As well the location of the commonly used interfaces as the mechanical specifications of the connectors are clearly defined.

The first connector X1 is called phyFLEX-fix connector. All phyFLEX SOMs support all interfaces specified for this connector at the same locations. The second connector X2, called phyFLEX-optional connector, has optional, but defined interfaces at fixed positions (e.g. SATA, CAN, camera). phyFLEX SOMs can, but do not have to support the interfaces at the phyFLEX-optional connector. The third connector, phyFLEX-flex connector X3, has only fixed Ground signals. All other signals of the phyFLEX-flex connector are module specific and depend on the features of the controller populating the SOM.

The numbering scheme for the phyFLEX-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number with prefixed Connector Reference (X1=phyFLEX-fix, X2=phyFLEX-optional, X3=phyFLEX-flex). Pin X1A1, for example, is always located in the upper left hand corner of the matrix of connector X1. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (refer to *Figure 4*).

The numbered matrix can be aligned with the phyFLEX-i.MX 6 (viewed from above; phyFLEX-Connector pointing down) or with the socket of the corresponding phyFLEX Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin X1A1) is thus covered with the corner of the phyFLEX-i.MX 6. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyFLEX-Connector as well as the mating connector on the phyFLEX Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

The following figure illustrates the numbered matrix system. It shows a phyFLEX-i.MX 6 with all three SMT phyFLEX-Connectors on its underside (defined as dotted lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyFLEX-i.MX 6 module showing the phyFLEX-Connector mounted on the underside of the module's PCB.

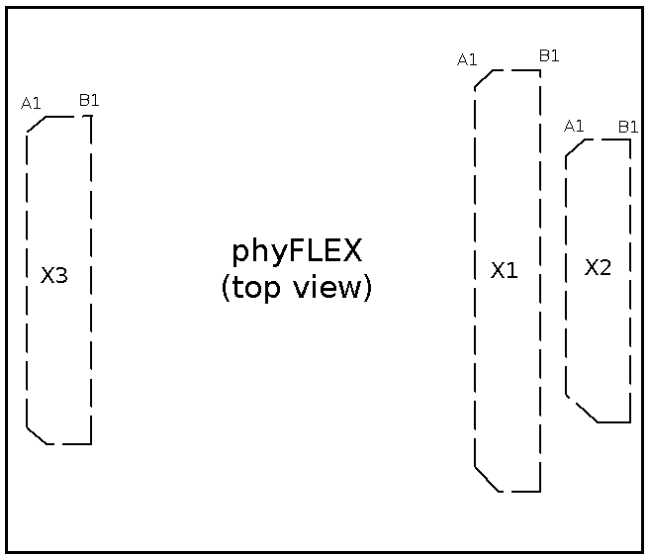

Figure 4: Pinout of the phyFLEX-Connector (top view)

Table 3 to *Table 8* provide an overview of the pinout of the different phyFLEX-Connectors X1, X2, and X3 with signal names and descriptions specific to the phyFLEX-i.MX 6. It also provides the appropriate voltage domain, signal type (ST) and a functional grouping of the signals. The signal type includes also information about the signal[1]. A description of the signal types can be found in *Table 1*.

The Freescale Semiconductor i.MX 6 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Freescale Semiconductor i.MX 6 Reference Manual* for details on the functions and features of controller signals and port pins.

[1]: The specified direction indicated refers to the standard phyFLEX use of the pin.

Pin #	Signal	ST	Voltage domain	Description
X1A1	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A2	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A3	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A4	GND	-	-	Ground 0 V
X1A5	X_JTAG_TRSTB	I	VDD_3V3_LOGIC	JTAG reset input (low active)
X1A6	X_JTAG_TDI	I	VDD_3V3_LOGIC	JTAG TDI
X1A7	X_JTAG_TMS	I	VDD_3V3_LOGIC	JTAG TMS
X1A8	X_JTAG_TDO	O	VDD_3V3_LOGIC	JTAG TDO
X1A9	X_JTAG_TCK	I	VDD_3V3_LOGIC	JTAG clock input
X1A10	GND	-	-	Ground 0 V
X1A11	N.C.	-	-	Not connected
X1A12	X_UART1_TxD_TTL	O	VDD_3V3_LOGIC	UART1 serial transmit signal
X1A13	X_UART1_RxD_TTL	I	VDD_3V3_LOGIC	UART1 serial data receive signal
X1A14	X_UART1_RTS_TTL	O	VDD_3V3_LOGIC	UART1 request to send
X1A15	X_UART1_CTS_TTL	I	VDD_3V3_LOGIC	UART1 clear to send
X1A16	GND	-	-	Ground 0 V
X1A17	reference-voltage	REF_O	VDD_3V3_LOGIC	UART1 reference voltage
X1A18	X_UART0_TxD_TTL	O	VDD_3V3_LOGIC	UART0 serial transmit signal
X1A19	reference-voltage	REF_O	VDD_3V3_LOGIC	UART0 reference voltage
X1A20	X_UART0_RxD_TTL	I	VDD_3V3_LOGIC	UART0 serial data receive signal
X1A21	X_SPI0_MOSI	O	VDD_3V3_LOGIC	SPI0 master output/slave input
X1A22	GND	-	-	Ground 0 V
X1A23	X_SPI0_MISO	I	VDD_3V3_LOGIC	SPI0 master input/slave output
X1A24	X_SPI0_CSBOOT	O	VDD_3V3_LOGIC	SPI0 Chip Select BOOT
X1A25	X_SPI0_CS0	O	VDD_3V3_LOGIC	SPI0 Chip Select 0
X1A26	X_SPI0_CS1	O	VDD_3V3_LOGIC	SPI0 Chip Select 1
X1A27	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI0 reference voltage
X1A28	GND	-	-	Ground 0 V
X1A29	X_SPI0_CLK	O	VDD_3V3_LOGIC	SPI0 clock signal

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A

X1A30	X_SPI1_CS0[1]	O	VDD_3V3_LOGIC	SPI1 chip select 0
X1A31	X_SPI1_MOSI[1]	O	VDD_3V3_LOGIC	SPI1 master output/slave input
X1A32	X_SPI1_MISO[1]	I	VDD_3V3_LOGIC	SPI1 master input/slave output
X1A33	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI1 reference voltage
X1A34	GND	-	-	Ground 0 V
X1A35	X_SPI1_CLK[1]	O	VDD_3V3_LOGIC	SPI1 clock signal
X1A36	X_SPI1_CS1[1]	O	VDD_3V3_LOGIC	SPI1 chip select 1
X1A37	X_USB0_nVBUSEN	O	VDD_3V3_LOGIC	USB0 VBUS enable (active low)
X1A38	X_USB0_VBUS	PWR_I	5V	USB0 VBUS input
X1A39	X_USB0_nOC	IPU	VDD_3V3_LOGIC	USB0 overcurrent input
X1A40	GND	-	-	Ground 0 V
X1A41	reference-voltage	REF_O	VDD_3V3_LOGIC	USB0 reference voltage
X1A42	X_USB0_CHGDET	O	VDD_3V3_LOGIC	USB0 charger detection
X1A43	X_USB1_nVBUSEN	O	VDD_3V3_LOGIC	USB1 VBUS enable (active low)
X1A44	X_USB1_VBUS	PWR_I	5V	USB1 VBUS input
X1A45	X_USB1_nOC	IPU	VDD_3V3_LOGIC	USB1 overcurrent input
X1A46	GND	-	-	Ground 0 V
X1A47	reference-voltage	REF_O	VDD_3V3_LOGIC	USB1 reference voltage
X1A48	X_I2S0_CLK	O	VDD_3V3_LOGIC	I^2S receive clock
X1A49	X_I2S0_FRM	O	VDD_3V3_LOGIC	I^2S receive frame
X1A50	X_I2S0_ADC	I	VDD_3V3_LOGIC	I^2S receive data
X1A51	reference-voltage	REF_O	VDD_3V3_LOGIC	I^2S reference voltage
X1A52	GND	-	-	Ground 0 V
X1A53	X_I2S0_DAC	O	VDD_3V3_LOGIC	I^2S transmit data
X1A54	X_GPIO0	I/O	VDD_3V3_LOGIC	General purpose input/output 0
X1A55	X_GPIO1	I/O	VDD_3V3_LOGIC	General purpose input/output 1
X1A56	X_GPIO2	I/O	VDD_3V3_LOGIC	General purpose input/output 2
X1A57	reference-voltage	REF_O	VDD_3V3_LOGIC	GPIO reference voltage
X1A58	GND	-	-	Ground 0 V
X1A59	X_GPIO3	I/O	VDD_3V3_LOGIC	General purpose input/output 3
X1A60	X_GPIO4	I/O	VDD_3V3_LOGIC	General purpose input/output 4

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A (continued)

[1]: SPI1 is not available for i.MX 6 Solo and i.MX 6 Dual Lite

X1A61	X_GPIO5	I/O	VDD_3V3_LOGIC	General purpose input/output 5
X1A62	X_GPIO6	I/O	VDD_3V3_LOGIC	General purpose input/output 6
X1A63	X_GPIO7	I/O	VDD_3V3_LOGIC	General purpose input/output 7
X1A64	GND	-	-	Ground 0 V
X1A65	X_GPIO8	I/O	VDD_3V3_LOGIC	General purpose input/output 8
X1A66	X_GPIO9	I/O	VDD_3V3_LOGIC	General purpose input/output 9
X1A67	X_GPIO10	I/O	VDD_3V3_LOGIC	General purpose input/output 10
X1A68	X_I2C0_SDA	OC-BI	VDD_3V3_LOGIC	I2C0 data
X1A69	X_I2C0_SCL	OC-BI	VDD_3V3_LOGIC	I2C0 clock
X1A70	GND	-	-	Ground 0 V
X1A71	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C0 reference voltage
X1A72	X_PM_nRESET_IN	IPU	VDD_PM	Reset input
X1A73	X_PM_nRESET_OUT	OC	-	Reset output
X1A74	X_PM_SDA	OC-BI	VDD_3V3_LOGIC	Power management bus data (EMIC)
X1A75	X_PM_SCL	OC-BI	VDD_3V3_LOGIC	Power management bus clock (EMIC)
X1A76	GND	-	-	Ground 0 V
X1A77	X_PM_nON/WAKEUP/ OFF	IPU	VDD_PM	Power on/wakeup/power off input
X1A78	X_PM_PWR_GOOD	OC	-	Power good output
X1A79	X_PM_PWM	OC	-	Fan PWM output
X1A80	X_PM_TACHO	5V_PD	-	Fan tacho input

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B1	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B2	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B3	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B4	GND	-	-	Ground 0 V
X1B5	reference-voltage	REF_O	VDD_3V3_LOGIC	JTAG reference voltage
X1B6	RSVD	-	-	Reserved
X1B7	GND	-	-	Ground 0 V

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B

X1B8	reference-voltage	REF_O	VDD_SD0	SD0 reference voltage
X1B9	X_SD0_nWP	I	VDD_SD0	SD0 write protection (active low)
X1B10	X_SD0_nCD	I	VDD_SD0	SD0 card detection (active low)
X1B11	X_SD0_D3	I/O	VDD_SD0	SD0 data 3
X1B12	X_SD0_CMD	O	VDD_SD0	SD0 command
X1B13	GND	-	-	Ground 0 V
X1B14	X_SD0_CLK	O	VDD_SD0	SD0 clock
X1B15	X_SD0_D0	I/O	VDD_SD0	SD0 data 0
X1B16	X_SD0_D1	I/O	VDD_SD0	SD0 data 1
X1B17	X_SD0_D2	I/O	VDD_SD0	SD0 data 2
X1B18	X_SD0_D4	I/O	VDD_SD0	SD0 data 4
X1B19	GND	-	-	Ground 0 V
X1B20	X_SD0_D5	I/O	VDD_SD0	SD0 data 5
X1B21	X_SD0_D6	I/O	VDD_SD0	SD0 data 6
X1B22	X_SD0_D7	I/O	VDD_SD0	SD0 data 7
X1B23	RSVD	-	-	reserved
X1B24	X_ETH0_ANALOG_ VOLTAGE	REF_O	VDD_3V3_LOGIC	ETH0 reference voltage for 10/100 Mbit
X1B25	GND	-	-	Ground 0 V
X1B26	X_ETH0_A+/TX0+	ETH_O	VDD_3V3_LOGIC	ETH0 data A+ /transmit+
X1B27	X_ETH0_A-/TX0-	ETH_O	VDD_3V3_LOGIC	ETH0 data A-/transmit-
X1B28	X_ETH0_LED0	OC	VDD_3V3_LOGIC	ETH0 link LED output
X1B29	X_ETH0_B+/RX0+	ETH_I	VDD_3V3_LOGIC	ETH0 data B+/receive+
X1B30	X_ETH0_B-/RX0-	ETH_I	VDD_3V3_LOGIC	ETH0 data B-/receive-
X1B31	GND	-	-	Ground 0 V
X1B32	X_ETH0_C+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C+ (only GbE)
X1B33	X_ETH0_C-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C- (only GbE)
X1B34	X_ETH0_LED1	OC	VDD_3V3_LOGIC	ETH0 traffic LED output
X1B35	X_ETH0_D+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D+ (only GbE)
X1B36	X_ETH0_D-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D- (only GbE)
X1B37	GND	-	-	Ground 0 V
X1B38	X_USB0_D-	USB_I/O	i.MX 6 internal	USB0 data-
X1B39	X_USB0_D+	USB_I/O	i.MX 6 internal	USB0 data+
X1B40	X_USB0_ID	I	VDD_3V3_LOGIC	USB0 ID Pin
X1B41	N.C.	-	-	Not connected
X1B42	N.C.	-	-	Not connected
X1B43	GND	-	-	Ground 0 V
X1B44	X_USB1_D-	USB_/IO	i.MX 6 internal	USB0 data-
X1B45	X_USB1_D+	USB_I/O	i.MX 6 internal	USB0 data+

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B (continued)

X1B46	RSVD	-	-	reserved
X1B47	N.C.	-	-	Not connected
X1B48	N.C.	-	-	Not connected
X1B49	GND		-	Ground 0 V
X1B50	X_LVDS0_L0+	LVDS_O	i.MX 6 internal	LVDS0 data0+
X1B51	X_LVDS0_L0-	LVDS_O	i.MX 6 internal	LVDS0 data0-
X1B52	X_LVDS0_nDISP_EN	I/O	VDD_3V3_LOGIC	LVDS0 display enable (low active)
X1B53	X_LVDS0_L1+	LVDS_O	i.MX 6 internal	LVDS0 data1+
X1B54	X_LVDS0_L1-	LVDS_O	i.MX 6 internal	LVDS0 data1-
X1B55	GND	-	-	Ground 0 V
X1B56	X_LVDS0_L2+	LVDS_O	i.MX 6 internal	LVDS0 data2+
X1B57	X_LVDS0_L2-	LVDS_O	i.MX 6 internal	LVDS0 data2-
X1B58	X_LVDS0_DISP_BL_PWM	I/O	VDD_3V3_LOGIC	LVDS0 backlight PWM output
X1B59	X_LVDS0_L3+	LVDS_O	i.MX 6 internal	LVDS0 data3+
X1B60	X_LVDS0_L3-	LVDS_O	i.MX 6 internal	LVDS0 data3-
X1B61	GND	-	-	Ground 0 V
X1B62	X_LVDS0_CLK+	LVDS_O	i.MX 6 internal	LVDS0 clock+
X1B63	X_LVDS0_CLK-	LVDS_O	i.MX 6 internal	LVDS0 clock-
X1B64	reference-voltage	REF_O	VDD_3V3_LOGIC	LVDS0 reference voltage
X1B65	X_PCIe0_nPRSNT	I/O	VDD_3V3_LOGIC	PCIe0 present signal (low active)
X1B66	reference-voltage	REF_O	VDD_3V3_LOGIC	PCIe0 reference voltage
X1B67	GND	-	-	Ground 0 V
X1B68	X_PCIe0_TX+	PCIe_O	i.MX 6 internal	PCIe0 transmit lane+
X1B69	X_PCIe0_TX-	PCIe_O	i.MX 6 internal	PCIe0 transmit lane-
X1B70	X_PCIe0_nWAKE	I/O	VDD_3V3_LOGIC	PCIe0 wake signal (low active)
X1B71	X_PCIe0_RX+	PCIe_I	i.MX 6 internal	PCIe0 receive lane+
X1B72	X_PCIe0_RX-	PCIe_I	i.MX 6 internal	PCIe0 receive lane-
X1B73	GND	-	-	Ground 0 V
X1B74	X_PCIe0_CLK+	PCIe_O	i.MX 6 internal	PCIe0 clock lane+
X1B75	X_PCIe0_CLK-	PCIe_O	i.MX 6 internal	PCIe0 clock lane-
X1B76	X_BOOT0	IPU	VDD_PM	Boot configuration 0
X1B77	X_BOOT1	IPU	VDD_PM	Boot configuration 1
X1B78	X_BOOT2	IPU	VDD_PM	Boot configuration 2
X1B79	GND	-	-	Ground 0 V
X1B80	RSVD	-	-	reserved

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2A1	X_I2C1_SDA	OC-BI	VDD_3V3_LOGIC	I2C1 data
X2A2	X_I2C1_SCL	OC-BI	VDD_3V3_LOGIC	I2C1 clock
X2A3	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C1 reference voltage
X2A4	X_CAN0_TXD	O	VDD_3V3_LOGIC	CAN0 transmit
X2A5	X_CAN0_RXD	I	VDD_3V3_LOGIC	CAN0 receive
X2A6	GND	-	-	Ground 0 V
X2A7	reference-voltage	REF_O	VDD_3V3_LOGIC	CAN0 reference voltage
X2A8	X_HDMI0_SDA	I/O	VDD_3V3_LOGIC	HDMI0 I^2C data
X2A9	X_HDMI0_SCL	I/O	VDD_3V3_LOGIC	HDMI0 I^2C clock
X2A10	X_SATA0_TX+	LVDS_O	i.MX 6 internal	SATA0 transmit lane+
X2A11	X_SATA0_TX-	LVDS_O	i.MX 6 internal	SATA0 transmit lane-
X2A12	GND	-	-	Ground 0 V
X2A13	X_SATA0_RX+	LVDS_I	i.MX 6 internal	SATA0 receive lane+
X2A14	X_SATA0_RX-	LVDS_I	i.MX 6 internal	SATA0 receive lane-
X2A15	X_SD1_D3	I/O	VDD_SD1	SD1 data 3
X2A16	X_SD1_CMD	O	VDD_SD1	SD1 command
X2A17	X_SD1_CLK	O	VDD_SD1	SD1 clock
X2A18	GND	-	-	Ground 0 V
X2A19	reference-voltage	REF_O	VDD_SD1	SD1 reference voltage
X2A20	X_SD1_nWP	I	VDD_SD1	SD1 write protection (active low)
X2A21	X_SD1_nCD	I	VDD_SD1	SD1 card detection (active low)
X2A22	X_SD1_D0	I/O	VDD_SD1	SD1 data 0
X2A23	X_SD1_D1	I/O	VDD_SD1	SD1 data 1
X2A24	GND	-	-	Ground 0 V
X2A25	X_SD1_D2	I/O	VDD_SD1	SD1 data 2
X2A26	N.C.	-	-	Not connected
X2A27	N.C.	-	-	Not connected
X2A28	N.C.	-	-	Not connected
X2A29	N.C.	-	-	Not connected
X2A30	GND	-	-	Ground 0 V
X2A31	N.C.	-	-	Not connected
X2A32	N.C.	-	-	Not connected
X2A33	N.C.	-	-	Not connected
X2A34	N.C.	-	-	Not connected
X2A35	N.C.	-	-	Not connected
X2A36	GND	-	-	Ground 0 V
X2A37	N.C.	-	-	Not connected

Table 5: Pinout of the phyFLEX-optional Connector X2, Row A

X2A38	N.C.	-	-	Not connected
X2A39	N.C.	-	-	Not connected
X2A40	X_CAMERA0_L0+	LVDS_I	VDD_3V3_LOGIC	Camera0 data+
X2A41	X_CAMERA0_L0-	LVDS_I	VDD_3V3_LOGIC	Camera0 data-
X2A42	GND	-	-	Ground 0 V
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera0 master clock
X2A44	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera0 reference voltage
X2A45	RSVD	-	-	reserved
X2A46	X_CAMERA1_L0+	LVDS_I	VDD_3V3_LOGIC	Camera1 data+
X2A47	X_CAMERA1_L0-	LVDS_I	VDD_3V3_LOGIC	Camera1 data-
X2A48	GND	-	-	Ground 0 V
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera1 master clock
X2A50	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera1 reference voltage

Table 5: Pinout of the phyFLEX-optional Connector X2, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2B1	X_HDMI0_TMDS_DATA2+	TMDS_O	i.MX 6 internal	HDMI0 data2+
X2B2	X_HDMI0_TMDS_DATA2-	TMDS_O	i.MX 6 internal	HDMI0 data2-
X2B3	GND	-	-	Ground 0 V
X2B4	X_HDMI0_TMDS_DATA1+	TMDS_O	i.MX 6 internal	HDMI0 data1+
X2B5	X_HDMI0_TMDS_DATA1-	TMDS_O	i.MX 6 internal	HDMI0 data1-
X2B6	reference-voltage	REF_O	VDD_3V3_LOGIC	HDMI0 reference voltage
X2B7	X_HDMI0_TMDS_DATA0+	TMDS_O	i.MX 6 internal	HDMI0 data0+
X2B8	X_HDMI0_TMDS_DATA0-	TMDS_O	i.MX 6 internal	HDMI0 data0-
X2B9	GND	-	-	Ground 0 V
X2B10	X_HDMI0_TMDS_CLOCK+	TMDS_O	i.MX 6 internal	HDMI0 clock+
X2B11	X_HDMI0_TMDS_CLOCK-	TMDS_O	i.MX 6 internal	HDMI0 clock-
X2B12	X_HDMI0_CEC	I/O	VDD_3V3_LOGIC	HDMI0 CEC
X2B13	X_HDMI0_nHPD	I	VDD_3V3_LOGIC	HDMI0 hot plug detect
X2B14	N.C.	-	-	Not connected
X2B15	GND	-	-	Ground 0 V
X2B16	N.C.	-	-	Not connected

Table 6: Pinout of the phyFLEX-optional Connector X2, Row B

X2B17	N.C.	-	-	Not connected
X2B18	N.C.	-	-	Not connected
X2B19	N.C.	-	-	Not connected
X2B20	N.C.	-	-	Not connected
X2B21	GND	-	-	Ground 0 V
X2B22	N.C.	-	-	Not connected
X2B23	N.C.	-	-	Not connected
X2B24	N.C.	-	-	Not connected
X2B25	N.C.	-	-	Not connected
X2B26	N.C.	-	-	Not connected
X2B27	GND	-	-	Ground 0 V
X2B28	N.C.	-	-	Not connected
X2B29	N.C.	-	-	Not connected
X2B30	RSVD	-	-	reserved
X2B31	N.C.	-	-	Not connected
X2B32	N.C.	-	-	Not connected
X2B33	GND	-	-	Ground 0 V
X2B34	N.C.	-	-	Not connected
X2B35	N.C.	-	-	Not connected
X2B36	RSVD	-	-	reserved
X2B37	N.C.	-	-	Not connected
X2B38	N.C.	-	-	Not connected
X2B39	GND	-	-	Ground 0 V
X2B40	N.C.	-	-	Not connected
X2B41	N.C.	-	-	Not connected
X2B42	RSVD	-	-	reserved
X2B43	N.C.	-	-	Not connected
X2B44	N.C.	-	-	Not connected
X2B45	GND	-	-	Ground 0 V
X2B46	N.C.	-	-	Not connected
X2B47	N.C.	-	-	Not connected
X2B48	N.C.	-	-	Not connected
X2B49	N.C.	-	-	Not connected
X2B50	N.C.	-	-	Not connected

Table 6: Pinout of the phyFLEX-optional Connector X2, Row B (continued)

Note: Signals on the phyFLEX-fix (X1) and phyFLEX-optional (X2) connectors have fixed positions equal for all phyFLEX SOMs. Furthermore all phyFLEX SOMs support all interfaces specified for the phyFLEX-fix connector (X1). As opposed to this, the phyFLEX-optional connector (X2) has optional, but defined interfaces at fixed

positions (e.g. SATA, CAN, camera). Other phyFLEX SOMs might have more, or less interfaces.

Pin #	Signal	ST	Voltage Domain	Description
X3A1	X_CSI_CLK0P	CSI-2_I	i.MX 6 internal	CSI clock+
X3A2	X_CSI_CLK0M	CSI-2_I	i.MX 6 internal	CSI clock-
X3A3	X_CSI0_DAT10	I	VDD_3V3_LOGIC	CSI0 data10
X3A4	X_CSI_D0P	CSI-2_I	i.MX 6 internal	CSI data0+
X3A5	X_CSI_D0M	CSI-2_I	i.MX 6 internal	CSI data0-
X3A6	GND	-	-	Ground 0 V
X3A7	X_CSI_D1P	CSI-2_I	i.MX 6 internal	CSI data1+
X3A8	X_CSI_D1M	CSI-2_I	i.MX 6 internal	CSI data1-
X3A9	X_CSI0_DAT11	I	VDD_3V3_LOGIC	CSI0 data11
X3A10	X_CSI_D2P	CSI-2_I	i.MX 6 internal	CSI data2+
X3A11	X_CSI_D2M	CSI-2_I	i.MX 6 internal	CSI data2-
X3A12	GND	-	-	Ground 0 V
X3A13	X_CSI_D3P	CSI-2_I	i.MX 6 internal	CSI data3+
X3A14	X_CSI_D3M	CSI-2_I	i.MX 6 internal	CSI data3-
X3A15	X_CSI0_DAT12	I	VDD_3V3_LOGIC	CSI0 data12
X3A16	X_CSI0_DAT13	I	VDD_3V3_LOGIC	CSI0 data13
X3A17	X_CSI0_DAT14	I	VDD_3V3_LOGIC	CSI0 data14
X3A18	GND	-	-	Ground 0 V
X3A19	X_CSI0_DAT15	I	VDD_3V3_LOGIC	CSI0 data15
X3A20	X_CSI0_DAT16	I	VDD_3V3_LOGIC	CSI0 data16
X3A21	X_CSI0_DAT17	I	VDD_3V3_LOGIC	CSI0 data17
X3A22	X_CSI0_DAT18	I	VDD_3V3_LOGIC	CSI0 data18
X3A23	X_CSI0_DAT19	I	VDD_3V3_LOGIC	CSI0 data19
X3A24	GND	-	-	Ground 0 V
X3A25	X_CSI0_MCLK	O	VDD_3V3_LOGIC	CSI0 master clock
X3A26	X_CSI0_PIXCLK	O	VDD_3V3_LOGIC	CSI0 pixel clock
X3A27	X_CSI0_VSYNC	I	VDD_3V3_LOGIC	CSI0 vertical sync
X3A28	X_CSI0_DATA_EN	O	VDD_3V3_LOGIC	CSI0 data enable
X3A29	X_TAMPER	I	VDD_3V3_LOGIC	Tamper
X3A30	GND	-	-	Ground 0 V
X3A31	X_EIM_WAIT	I	VDD_3V3_LOGIC	EIM wait
X3A32	X_EIM_A24	O	VDD_3V3_LOGIC	EIM address24
X3A33	X_EIM_A23	O	VDD_3V3_LOGIC	EIM address23
X3A34	X_EIM_A22	O	VDD_3V3_LOGIC	EIM address22
X3A35	X_EIM_A21	O	VDD_3V3_LOGIC	EIM address21

Table 7: Pinout of the phyFLEX-flex Connector X3, Row A

X3A36	GND	-	-	Ground 0 V
X3A37	X_EIM_A20	O	VDD_3V3_LOGIC	EIM address20
X3A38	X_EIM_A19	O	VDD_3V3_LOGIC	EIM address19
X3A39	X_EIM_A18	O	VDD_3V3_LOGIC	EIM address18
X3A40	X_EIM_A17	O	VDD_3V3_LOGIC	EIM address17
X3A41	X_EIM_EB0	O	VDD_3V3_LOGIC	EIM enable byte0
X3A42	GND	-	-	Ground 0 V
X3A43	X_EIM_EB1	O	VDD_3V3_LOGIC	EIM enable byte1
X3A44	X_EIM_DA0	I/O	VDD_3V3_LOGIC	EIM address/data0
X3A45	X_EIM_DA1	I/O	VDD_3V3_LOGIC	EIM address/data1
X3A46	X_EIM_DA2	I/O	VDD_3V3_LOGIC	EIM address/data2
X3A47	X_EIM_DA3	I/O	VDD_3V3_LOGIC	EIM address/data3
X3A48	GND	-	-	Ground 0 V
X3A49	X_EIM_DA4	I/O	VDD_3V3_LOGIC	EIM address/data4
X3A50	X_EIM_DA5	I/O	VDD_3V3_LOGIC	EIM address/data5
X3A51	X_EIM_DA6	I/O	VDD_3V3_LOGIC	EIM address/data6
X3A52	X_EIM_DA7	I/O	VDD_3V3_LOGIC	EIM address/data7
X3A53	X_EIM_DA8	I/O	VDD_3V3_LOGIC	EIM address/data8
X3A54	GND	-	-	Ground 0 V
X3A55	X_EIM_DA9	I/O	VDD_3V3_LOGIC	EIM address/data9
X3A56	X_EIM_DA10	I/O	VDD_3V3_LOGIC	EIM address/data10
X3A57	X_EIM_DA11	I/O	VDD_3V3_LOGIC	EIM address/data11
X3A58	X_EIM_DA12	I/O	VDD_3V3_LOGIC	EIM address/data12
X3A59	X_EIM_A16	O	VDD_3V3_LOGIC	EIM address16
X3A60	GND	-	-	Ground 0 V

Table 7: Pinout of the phyFLEX-flex Connector X3, Row A (continued)

Pin #	Signal	ST	Votlage domain	Description
X3B1	X_LVDS1_TX0_P	LVDS_O	i.MX 6 internal	LVDS1 data0+
X3B2	X_LVDS1_TX0_N	LVDS_O	i.MX 6 internal	LVDS1 data0-
X3B3	GND	-	-	Ground 0 V
X3B4	X_LVDS1_TX1_P	LVDS_O	i.MX 6 internal	LVDS1 data1+
X3B5	X_LVDS1_TX1_N	LVDS_O	i.MX 6 internal	LVDS1 data1-
X3B6	X_DISP0_DAT9/PWM2_PWMO	O	VDD_3V3_LOGIC	DISP0 data9/PWM2 output
X3B7	X_LVDS1_TX2_P	LVDS_O	i.MX 6 internal	LVDS1 data2+
X3B8	X_LVDS1_TX2_N	LVDS_O	i.MX 6 internal	LVDS1 data2-
X3B9	GND	-	-	Ground 0 V
X3B10	X_LVDS1_TX3_P	LVDS_O	i.MX 6 internal	LVDS1 data3+
X3B11	X_LVDS1_TX3_N	LVDS_O	i.MX 6 internal	LVDS1 data3-

Table 8: Pinout of the phyFLEX-flex Connector X3, Row B

X3B12	X_CSI0_DAT4	I	VDD_3V3_LOGIC	CSI0 data4
X3B13	X_LVDS1_CLK_P	LVDS_O	i.MX 6 internal	LVDS1 clock+
X3B14	X_LVDS1_CLK_N	LVDS_O	i.MX 6 internal	LVDS1 clock-
X3B15	GND	-	-	Ground 0 V
X3B16	X_MLB_DP	MLB_I/O	i.MX 6 internal	Media local bus data line+
X3B17	X_MLB_DN	MLB_I/O	i.MX 6 internal	Media local bus data line-
X3B18	X_CSI0_DAT5	I	VDD_3V3_LOGIC	CSI0 data5
X3B19	X_MLB_SP	MLB_I/O	i.MX 6 internal	Media local bus signal line+
X3B20	X_MLB_SN	MLB_I/O	i.MX 6 internal	Media local bus signal line-
X3B21	GND	-	-	Ground 0 V
X3B22	X_MLB_CP	MLB_O	i.MX 6 internal	Media local bus clock+
X3B23	X_MLB_CN	MLB_O	i.MX 6 internal	Media local bus clock-
X3B24	X_CSI0_DAT9	I	VDD_3V3_LOGIC	CSI0 data9
X3B25	X_EIM_LBA	O	VDD_3V3_LOGIC	EIM load burst address
X3B26	X_EIM_RW	O	VDD_3V3_LOGIC	EIM Read/write
X3B27	GND	-	-	Ground 0 V
X3B28	X_CSI0_DAT8	I	VDD_3V3_LOGIC	CSI0 data8
X3B29	X_EIM_OE	O	VDD_3V3_LOGIC	EIM output enable
X3B30	X_EIM_BCLK	O	VDD_3V3_LOGIC	EIM burst clock
X3B31	X_EIM_DA13	I/O	VDD_3V3_LOGIC	EIM address/data13
X3B32	X_EIM_DA14	I/O	VDD_3V3_LOGIC	EIM address/data14
X3B33	GND	-	-	Ground 0 V
X3B34	X_EIM_DA15	I/O	VDD_3V3_LOGIC	EIM address/data15
X3B35	X_CLK2_P	LVDS_I/O	i.MX 6 internal	Differential clock2+
X3B36	X_CLK2_N	LVDS_I/O	i.MX 6 internal	Differential clock2-
X3B37	X_GPIO_16	I/O	VDD_3V3_LOGIC	GPIO16
X3B38	X_EIM_D22	I/O	VDD_3V3_LOGIC	EIM data22
X3B39	GND	-	-	Ground 0 V
X3B40	X_CSI0_DAT7	I	VDD_3V3_LOGIC	CSI0 data7
X3B41	X_CSI0_DAT6	I	VDD_3V3_LOGIC	CSI0 data6
X3B42	X_KEY_COL1	I/O	VDD_3V3_LOGIC	Keypad column1
X3B43	X_KEY_ROW1	I/O	VDD_3V3_LOGIC	Keypad row1
X3B44	PMIC_VBBAT	PWR_I	2V – 5V	PMIC Backup power supply
X3B45	GND	-	-	Ground 0 V
X3B46	VDD_MX6_SNVS	PWR_I	3V	i.MX6 Backup power supply (normally generated by PMIC)

Table 8: Pinout of the phyFLEX-flex Connector X3, Row B (continued)

X3B47	X_DI0_DISP_CLK	O	VDD_3V3_LOGIC	DI0 display clock
X3B48	X_DI0_PIN4	O	VDD_3V3_LOGIC	DI0 pin4
X3B49	X_DISP0_DAT6	O	VDD_3V3_LOGIC	DISP0 data6
X3B50	X_DISP0_DAT7	O	VDD_3V3_LOGIC	DISP0 data7
X3B51	GND	-	-	Ground 0 V
X3B52	X_DISP0_DAT10	O	VDD_3V3_LOGIC	DISP0 data10
X3B53	X_DISP0_DAT11	O	VDD_3V3_LOGIC	DISP0 data11
X3B54	X_DISP0_DAT12	O	VDD_3V3_LOGIC	DISP0 data12
X3B55	X_DISP0_DAT15	O	VDD_3V3_LOGIC	DISP0 data15
X3B56	X_DISP0_DAT20	O	VDD_3V3_LOGIC	DISP0 data20
X3B57	GND	-	-	Ground 0 V
X3B58	X_DISP0_DAT21	O	VDD_3V3_LOGIC	DISP0 data21
X3B59	X_DISP0_DAT22	O	VDD_3V3_LOGIC	DISP0 data22
X3B60	X_DISP0_DAT23	O	VDD_3V3_LOGIC	DISP0 data23

Table 8: Pinout of the phyFLEX-flex Connector X3, Row B (continued)

Caution! Signals on the phyFLEX-optional connector (X3) are module specific. This connector has only fixed Ground signals. All other signals of the phyFLEX-flex connector depend on the features of the controller populating the SOM.

3 Jumpers

For configuration purposes, the phyFLEX-i.MX 6 has several solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. *Table 9* below provides a functional summary of the solder jumpers which can be changed to adapt the phyFLEX-i.MX 6 to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyFLEX-i.MX 6.

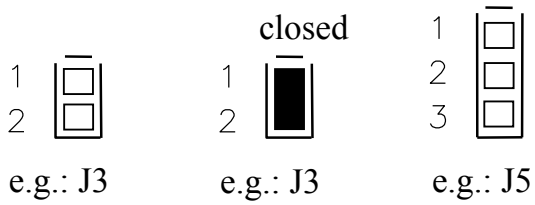

Figure 5: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Please pay special attention to the “TYPE” column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc…). The jumpers are either 0805 package or 0402 package with a 1/8 W or better power rating.

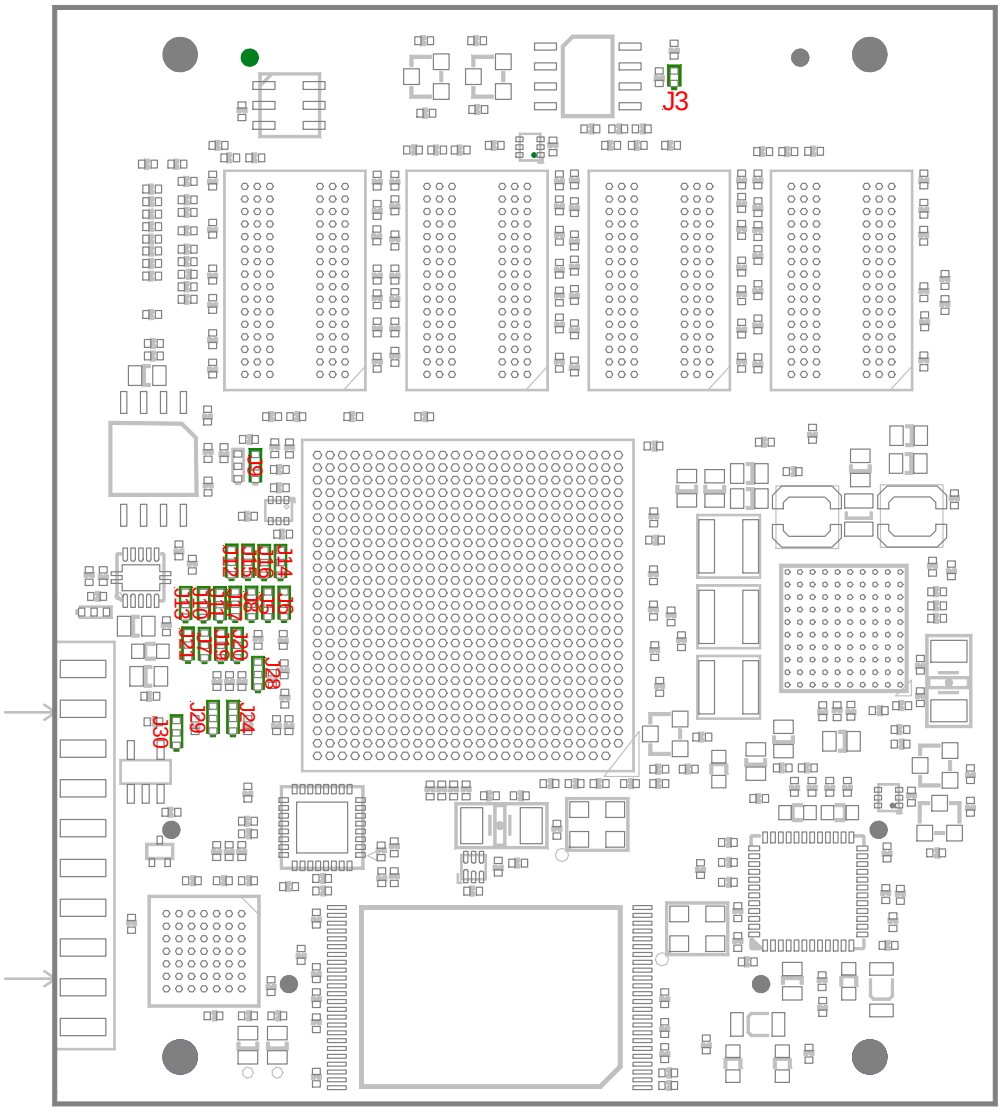

Figure 6: Jumper Locations (top view)

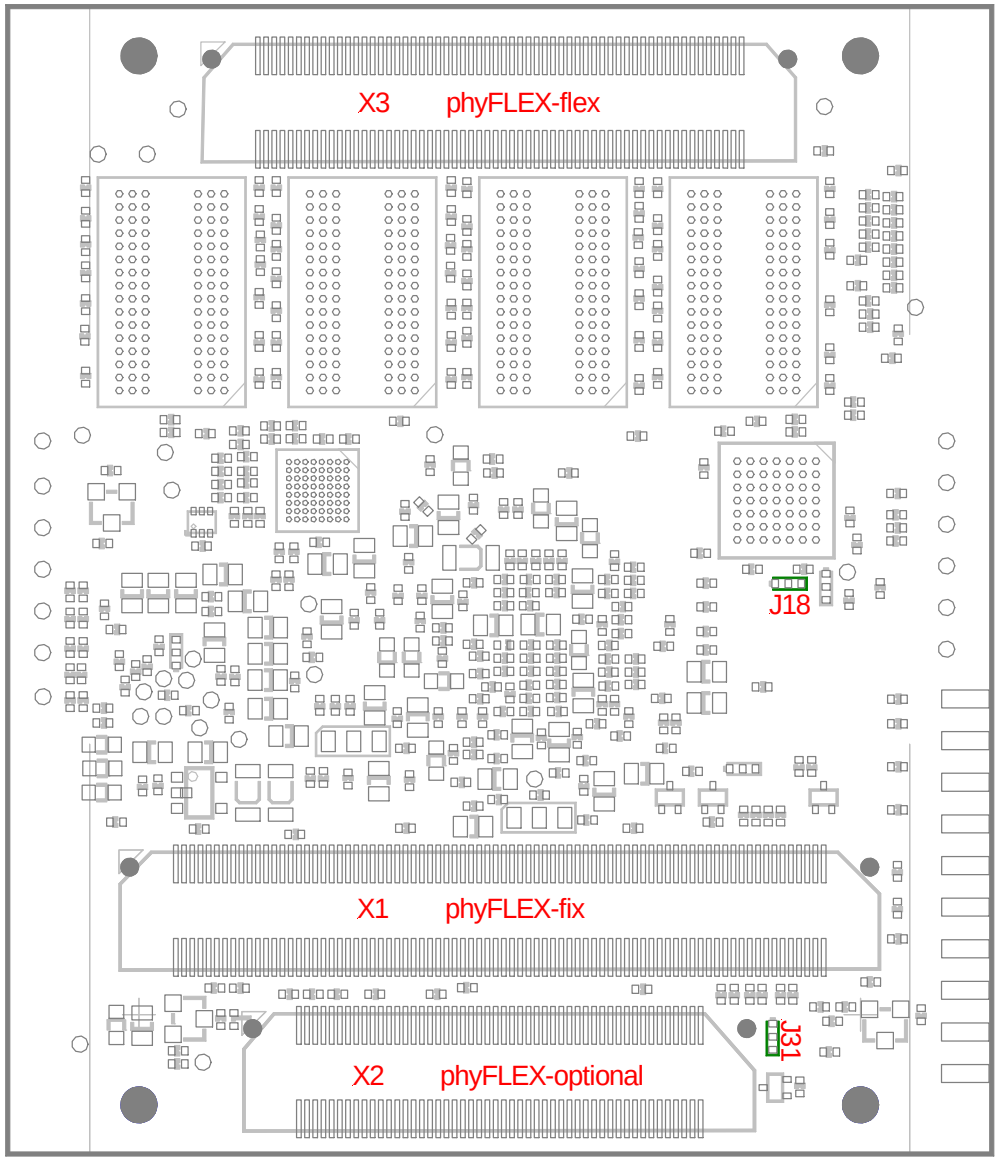

Figure 7: Jumper Locations (bottom view)

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J3	J3 connects the write protect input of the on board EEPROM with GND. If this jumper is not populated, the EEPROM is write protected.	0R (0402)	*6.3*
closed	**EEPROM is not write protected**		
open	EEPROM is write protected. The protection can be changed by the EEPROM_WP signal		
J5-J8, J10-J21, J24,J28-J30	These jumpers are connected to the boot configuration inputs of the i.MX 6. They can be used to change the boot settings according to the i.MX 6 datasheet. *Please refer to the i.MX 6 data sheet for more detailed information.*	10 kΩ (0402)	*5*
J9	J9 selects rising, or falling edge strobe for the LVDS Deserializer at U12 used for the camera connectivity of the phyFLEX-i.MX 6 (CSI1)	0 Ω (0402)	*14.1*
2+3	**rising edge strobe used for the LVDS camera signals**		
1+2	falling edge strobe used for the LVDS camera signals		
J31	J31 selects rising, or falling edge strobe for the LVDS Deserializer at U27 used for the camera connectivity of the phyFLEX-i.MX 6 (CSI0)	0 Ω (0402)	*14.1*
2+3	**rising edge strobe used for the LVDS camera signals**		
1+2	falling edge strobe used for the LVDS camera signals		

Table 9: Jumper Settings[2]

[2]: Default settings are in **bold blue** text

4 Power

The phyFLEX-i.MX 6 operates off of a single power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyFLEX-Connector X1 in detail.

4.1 Primary System Power (VDD_5V_IN_R)

The phyFLEX-i.MX 6 operates off of a primary voltage supply with a nominal value of +5 V. On-board switching regulators generate the 3.3 V, 2.5 V, 1.375 V, 1.5 V, 0.75 V, 1.2 V and 3 V voltage supplies required by the i.MX 6 MCU and on-board components from the primary 5 V supplied to the SOM.

For proper operation the phyFLEX-i.MX 6 must be supplied with a voltage source of 5 V ±5 % with 2 A load at the VCC pins on the phyFLEX-Connector X1.

VDD_5V_IN_R: X1 A1, A2, A3, B1, B2, B3

Connect all +5 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 A4, A10, A16, B4, B7, B13

Please refer to *section 2* for information on additional GND Pins located at the phyFLEX-Connector X1.

Caution:
As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

4.2 Power Management IC (PMIC) (U14)

The phyFLEX-i.MX 6 provides the on-board Power Management IC (PMIC) DA9063 at position U14 to generate different voltages required by the processor and the on-board components. *Figure 8* presents a graphical depiction of the powering scheme.

The DA9063 supports many functions like on-chip RTC and different power management functionalities like dynamic voltage control, different low power modes and regulator supervision. It is connected to the i.MX 6 via the on board I^2C bus. The I^2C address of the DA9063 is 0x58.

4.2.1 Power Domains

External voltages:

- VDD_5V_IN_R 5V main supply voltage
- USB0_VBUS USB0 Bus voltage, must be supplied with 5 V if USB0 is used
- USB1_VBUS USB1 Bus voltage, must be supplied with 5 V if USB1 is used
- PMIC_VBBAT PMIC Backup supply

Internal voltages:
VDD_5V_IN[3] : only used to generate other voltages

Internally generated voltages: VDD_MX6_ARM (1.375 V), VDD_MX6_SOC (1.375V), VDD_3V3_LOGIC (3.3 V), VDD_3V3_PMIC_IO (3.3V), VDD_SD0 and VDD_SD1 (3.3V), VDD_ETH_IO (2.5V) VDD_MX6_SNVS (3.0 V), VDD_MX6_HIGH (3.0V), VDD_PM (3.3 V), VDD_ETH_1V2 (1.2V), VDD_DDR3_1V5 (1.5 V), DDR3_VTT (0.75 V), DDR3_VREF (0.75 V)

- VDD_MX6_ARM: (1.375 V) i.MX 6 core (VDDARM_IN, VDDARM23_IN)
- VDD_MX6_SOC: (1.375 V) i.MX 6 SOC (VDDSOC_IN)
- VDD_MX6_HIGH: (3.0 V) i.MX 6 internal regulator (VDDHIGH_IN)
- VDD_MX6_SNVS: (3.0 V) i.MX 6 backup supply (VDD_SNVS_IN)
- VDD_ETH_IO: (2.5 V) i.MX6 RGMII supply (NVCC_RGMII, NVCC_ENET), Ethernet PHY RGMII IO supply
- VDD_ETH_1V2: (1.2 V) Ethernet PHY core voltage

[3]: derived from 5V_IN_R via current sense amplifier at U16

- VDD_SD0: (3.3 V) — i.MX6 SD3 supply (NVCC_SD3)
- VDD_SD1: (3.3 V) — i.MX6 SD2 supply (NVCC_SD2)
- VDD_PM: (3.3 V) — CMIC supply
- VDD_3V3_PMIC_IO: (3.3 V) — PMIC IO supply
- VDD_DDR3_1V5: (1.5 V) — i.MX 6 DDR (NVCC_DRAM), RAM devices
- DDR3_VTT: (0.75 V) — RAM devices termination voltage
- DDR3_VREF: (0.75 V) — i.MX 6 DDR3 reference voltage (DRAM_VREF), RAM devices reference voltage
- VDD_3V3_LOGIC: (3.3 V) — i.MX 6 pad supply (NVCC_NANDF, NVCC_JTAG, NVCC_LCD, NVCC_CSI, NVCC_EIM, NVCC_GPIO), I2C EEPROM, SPI Flash, NAND Flash, Camera Deserializer, Ethernet PHY, EMIC

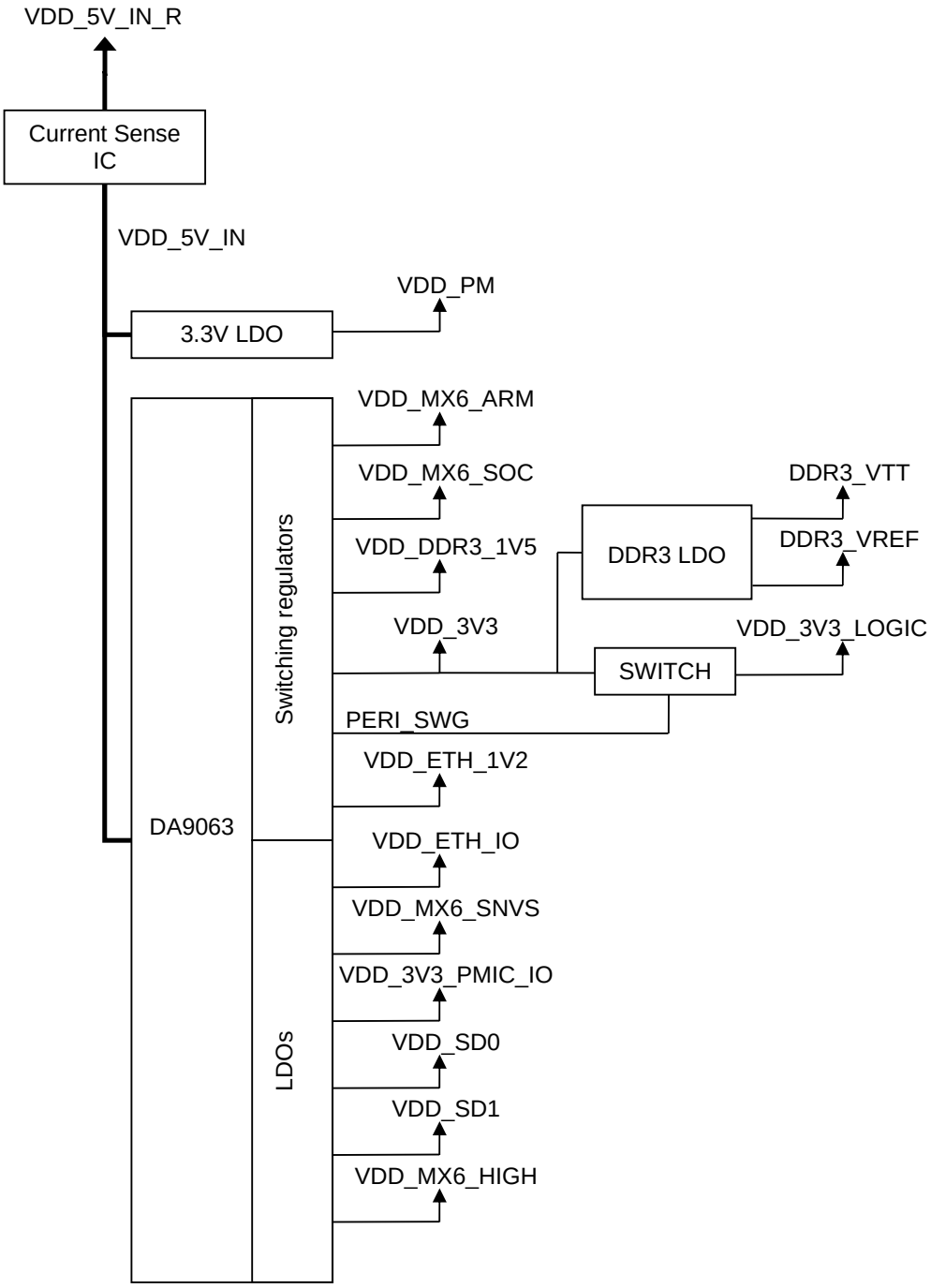

Figure 8: Powering scheme of phyFLEX- i.MX 6

4.3 Supply Voltage for external Logic

The voltage level of the phyFLEX's logic circuitry is VDD_3V3_LOGIC (3.3 V) which is generated on-board. In order to allow connecting external devices to the phyFLEX-i.MX 6 without the need of another voltage source in addition to the primary supply this voltage is brought out at the different reference voltage pins of the phyFLEX-Connector.

Use of level shifters supplied with VDD_3V3_LOGIC allows converting the signals according to the needs on the custom target hardware. Alternatively signals can be connected to an open drain circuitry with a pull-up resistor attached to VDD_3V3_LOGIC. Please use this voltage only as reference and not for supplying purpose.

4.4 Control Management IC (CMIC) (U17))

The phyFLEX-i.MX 6 provides an on-board Control Management IC (CMIC) at position U17 to control different phyFLEX specific functions such as power management, reset or boot configuration.

Please refer to the phyFLEX specification for further information.

5 System Configuration and Booting

Although most features of the i.MX 6 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Boot device order configuration

During the reset cycle the operational system boot mode of the i.MX 6 processor is determined by the configuration of two BOOTMODE pins BOOT_MODE[1:0]. These pins select the boot type. If the boot type is set to “Internal boot” (BOOT_MODE[1:0]=10, BOOT_CFGx[7:0] are used to configure further boot options. You can find further information about these boot pins in the *i.MX 6 Reference Manual*.

The internal ROM code is the first code executed during the initialization process of the i.MX 6 after POR. The ROM code detects which boot devices the controller has to check by using the BOOT_MODE[1:0] and particular BOOT_CFGx[7:0] pin configuration. For serial boot devices, the ROM code polls the communication interface selected, initiates the download of the code into the internal RAM and triggers its execution from there. For memory booting, the ROM code finds the bootstrap in permanent memories such as NAND-Flash or SD-Cards and executes it. Please refer to the *i.MX 6 Reference Manual* for more information.

The phyFLEX-i.MX 6 provides three boot configuration pins BOOT[2:0]. The setting of these pins configures the boot device which is selected by the processor. The standard phyFLEX boot options are shown in *Table 10*. Boot options specific for the i.MX 6 controller ar e shown in *Table 11*.

Boot Mode	X_BOOT2	X_BOOT1	X_BOOT0	Bootsource
0	1	1	1	On board memory (e.g. NAND, SSD, eMMC)
1 (optional)	1	1	0	SPI0
2 (optional)	1	0	1	alternative on board memory (e.g. SSD, eMMC)
3 (optional)	1	0	0	SD0 external
4 (optional)	0	1	1	Serial (UART or USB)
5 (optional)	0	1	0	SATA0
6 (optional)	0	0	1	USB0
7 (optional)	0	0	0	specific (e.g. PCIe, I2C, Ethernet……)

Table 10: Standard phyFLEX Boot Options

The phyFLEX-i.MX 6 specific boot options are shown in the following table.

Boot Mode	X_BOOT2	X_BOOT1	X_BOOT0	Bootsource
0	1	1	1	NAND
1	1	1	0	SPI3, CS0 (on board SPI Flash if populated, same as mode 2)
2	1	0	1	SPI3, CS0 (on board SPI Flash if populated, same as mode 1)
3	1	0	0	SD0 external
4	0	1	1	Serial USB OTG (USB0, same as mode 6)
5	0	1	0	SATA
6	0	0	1	Serial USB OTG (USB0, same as mode 4)
7	0	0	0	Bootconfig from eFUSE

Table 11: phyFLEX-i.MX 6 specific Boot Options

The BOOT[2:0] lines have 10 kΩ pull-up resistors populated on the module. Hence leaving the three pins unconnected sets the controller to boot mode 0, NAND boot.

Note:
As some of the signals which are brought out on the phyFLEX-flex connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals which may affect the boot configuration are shown in *Table 12*.

Pin #	Signal	I/O	SL	Description	Configuration Pin
X3A31	X_EIM_WAIT	I	3.3 V	EIM wait	BCFG4[1]
X3A32	X_EIM_A24	O	3.3 V	EIM address24	BCFG4[0]
X3A33	X_EIM_A23	O	3.3 V	EIM address23	BCFG3[7]
X3A34	X_EIM_A22	O	3.3 V	EIM address22	BCFG3[6]
X3A35	X_EIM_A21	O	3.3 V	EIM address21	BCFG3[5]
X3A37	X_EIM_A20	O	3.3 V	EIM address20	BCFG3[4]
X3A38	X_EIM_A19	O	3.3 V	EIM address19	BCFG3[3]
X3A39	X_EIM_A18	O	3.3 V	EIM address18	BCFG3[2]
X3A40	X_EIM_A17	O	3.3 V	EIM address17	BCFG3[1]
X3A41	X_EIM_EB0	O	3.3 V	EIM enable byte0	BCFG4[3]
X3A43	X_EIM_EB1	O	3.3 V	EIM enable byte1	BCFG4[4]
X3A44	X_EIM_DA0	I/O	3.3 V	EIM address/data0	BCFG1[0]
X3A45	X_EIM_DA1	I/O	3.3 V	EIM address/data1	BCFG1[1]
X3A46	X_EIM_DA2	I/O	3.3 V	EIM address/data2	BCFG1[2]
X3A47	X_EIM_DA3	I/O	3.3 V	EIM address/data3	BCFG1[3]
X3A49	X_EIM_DA4	I/O	3.3 V	EIM address/data4	BCFG1[4]
X3A50	X_EIM_DA5	I/O	3.3 V	EIM address/data5	BCFG1[5]
X3A51	X_EIM_DA6	I/O	3.3 V	EIM address/data6	BCFG1[6]
X3A52	X_EIM_DA7	I/O	3.3 V	EIM address/data7	BCFG1[7]
X3A53	X_EIM_DA8	I/O	3.3 V	EIM address/data8	BCFG2[0]
X3A55	X_EIM_DA9	I/O	3.3 V	EIM address/data9	BCFG2[1]
X3A56	X_EIM_DA10	I/O	3.3 V	EIM address/data10	BCFG2[2]

Table 12: Boot Configuration Pins at phyFLEX-flex Connector X3

Pin #	Signal	I/O	SL	Description	Configuration Pin
X3A57	X_EIM_DA11	I/O	3.3 V	EIM address/data11	BCFG2[3]
X3A58	X_EIM_DA12	I/O	3.3 V	EIM address/data12	BCFG2[4]
X3A59	X_EIM_A16	O	3.3 V	EIM address16	BCFG3[0]
X3B25	X_EIM_LBA	O	3.3 V	EIM load burst address	BCFG4[2]
X3B26	X_EIM_RW	O	3.3 V	EIM Read/write	BCFG4[5]
X3B31	X_EIM_DA13	I/O	3.3 V	EIM address/data13	BCFG2[5]
X3B32	X_EIM_DA14	I/O	3.3 V	EIM address/data14	BCFG2[6]
X3B34	X_EIM_DA15	I/O	3.3 V	EIM address/data15	BCFG2[7]

Table 12: Boot Configuration Pins at phyFLEX-flex Connector X3 (continued)

By setting the desired boot mode with the phyFLEX boot configuration pins BOOT[2:0], the CMIC, which is populated on the module, sets some of the appropriate BCFG pins and the BOOT_MODE[1:0] pins of the i.MX 6 controller. Only BCFG1[7:4], BCFG2[1], BCFG4[2] and BOOT_MODE[1:0] can be set by the CMIC. All other BCFG pins are set to a fixed value by 10 kΩ configuration resistors which are located on the phyFLEX module. Furthermore BCFG1[4], BCFG2[1] and BCFG4[2] have 10 kΩ on board configuration resistors, too.

The specific boot configuration settings, which are set by the on board configuration resistors, can be changed by modifying the resistors on the module or by connecting a configuration resistor (e.g. 1 kΩ) to the configuration signal. Please consider that any change of the default BCFG configuration can also influence other boot modes, which might result in faulty boot behavior.

For further information about the different boot modes and the influence of the BCFG pins please see the *i.MX 6 Reference Manual*.

Table 13 shows to which level the CMIC sets the different configuration signals for the boot modes. “Z” means that the CMIC sets the signal to high impedance, and thus the value of the configuration resistor is used.

Boot mode	Description	BOOT_MODE [1:0]	BCFG1[7:4]	BCFG2[1]	BCFG4[2]
0	NAND	0b10	0b1000	depends on NAND size	0bZ
1	SPI	0b10	0b0011	0bZ	0bZ
2	SPI	0b10	0b0011	0bZ	0bZ
3	SD0	0b10	0b010Z	0bZ	0bZ
4	USB OTG	0b01	0bZZZZ	0bZ	0bZ
5	SATA	0b10	0b0010	0bZ	0bZ
6	USB OTG	0b01	0bZZZZ	0bZ	0bZ
7	eFUSE	0b00	0bZZZZ	0bZ	0bZ

Table 13: Boot Configuration Signals generated by the CMIC

6 System Memory

The phyFLEX-i.MX 6 provides three types of on-board memory:

- 2 Banks DDR3 RAM: 1 GB DDR3 SDRAM (up to 4 GB)[4]
- NAND Flash (VFBGA): 1 GB (up to 16 GB)[1]
- I²C-EEPROM: 4 kB[1]
- SPI Flash: 16 MB[1]

The following sections of this chapter detail each memory type used on the phyFLEX-i.MX 6.

6.1 DDR3-SDRAM (U2-U9)

The RAM memory of the phyFLEX-i.MX 6 is comprised of up to two 64 bit wide banks each of four 16-bit wide DDR3-SDRAM chips (Bank 1: U2-U5, Bank 2: U6-U9). The chips are connected to the special DRR interface called Multi Mode DDR Controller (MMDC) of the i.MX 6 processor.

The DDR3 memory is accessed via the second AHB port starting at 0x1000 0000.

Typically the DDR3-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX 6 controller. Refer to the *i.MX 6 Reference Manual* for accessing and configuring these registers.

4: Please contact PHYTEC for more information about additional module configurations.

6.2 NAND Flash Memory (U13)

Use of Flash as non-volatile memory on the phyFLEX-i.MX 6 provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyFLEX-i.MX 6:

The Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

The NAND Flash memories are connected to the External Interface Module (EIM). /CS0 (NANDF_CS0) of the EIM interface selects the NAND Flash at U13.

6.3 I²C EEPROM (U10)

The phyFLEX-i.MX 6 is populated with a non-volatile 4 kB I[5] EEPROM with an I²C interface at U10. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 1 on the i.MX 6. The control registers for I²C port 1 are mapped between addresses 0x021A 0000 and 0x021A 3FFF. Please see the *i.MX 6 Reference Manual* for detailed information on the registers.
The three lower address bits are fixed to zero which means that the EEPROM can be accessed at I²C address 0x50.

Write protection to the device is accomplished via jumper J3. Refer to *section 6.3.1* for further details.

[5]: See the manufacturer's data sheet for interfacing and operation.

6.3.1 EEPROM Write Protection Control (J3)

Jumper J3 controls write access to the EEPROM (U10) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J3
Write access allowed	**closed**
Write protected	open

Table 14: EEPROM write protection states via J3[6]

Note: If the jumper is not set, the write protection signal can also be changed by GPIO3_19 of the i.MX 6 controller.

6.4 SPI Flash Memory (U25))

The optional SPI Flash Memory of the phyFLEX-i.MX 6 at U25 can be used to store configuration data or any other general purpose data. Beside this it can also be used as boot device. The device is accessed through eCSPI3 CS0 on the i.MX 6. The control registers for eCSPI3 are mapped between addresses 0x0201 0000 and 0x0201 3FFF. Please see the *i.MX 6 Reference Manual* for detailed information on the registers.

As of the printing of this manual these SPI Flash devices generally have a life expectancy of at least 100,000+ erase/program cycles and a data retention rate of 20 years. This makes the SPI Flash a reliable and secure solution to store the first and second level bootloaders.

6: Defaults are in **bold blue** text

7 SD / MMC Card Interfaces

The phyFLEX bus features one fixed and one optional SD / MMC Card interface. On the phyFLEX-i.MX 6 the interface signals extend from the controllers third and second Ultra Secured Digital (uSDHC3 / uSDHC2) Host Controller to the phyFLEX-Connector. *Table 15* shows the location of the different interface signals on the phyFLEX-Connector. The MMC/SD/SDIO Host Controller is fully compatible with the SD Memory Card Specification 3.0 and SD I/O Specification, Part E1, v1.10. SD / MMC Card interface SD0 (uSDHC3 of the i.MX 6), supports 8 data channels and SD1 (uSDHC2 of the i.MX 6) 4 data channels. Both interfaces have a maximum data rate of up to 104 MB/s (refer to the *i.MX 6 Reference Manual* for more information).

Pin #	Signal	ST	Voltage Domain	Description
X1B8	reference-voltage	REF_O	VDD_SD0	SD0 reference voltage
X1B9	X_SD0_nWP	I	VDD_SD0	SD0 write protect-tion (active low)
X1B10	X_SD0_nCD	I	VDD_SD0	SD0 card detection (active low)
X1B11	X_SD0_D3	I/O	VDD_SD0	SD0 data 3
X1B12	X_SD0_CMD	O	VDD_SD0	SD0 command
X1B13	GND	-	-	Ground 0 V
X1B14	X_SD0_CLK	O	VDD_SD0	SD0 clock
X1B15	X_SD0_D0	I/O	VDD_SD0	SD0 data 0
X1B16	X_SD0_D1	I/O	VDD_SD0	SD0 data 1
X1B17	X_SD0_D2	I/O	VDD_SD0	SD0 data 2
X1B18	X_SD0_D4	I/O	VDD_SD0	SD0 data 4
X1B20	X_SD0_D5	I/O	VDD_SD0	SD0 data 5
X1B21	X_SD0_D6	I/O	VDD_SD0	SD0 data 6

Table 15: Location of SD/ MMC Card Interface Signals

Pin #	Signal	ST	Voltage Domain	Description
X1B22	X_SD0_D7	I/O	VDD_SD0	SD0 data 7
X2A15	X_SD1_D3	I/O	VDD_SD1	SD1 data 3
X2A16	X_SD1_CMD	O	VDD_SD1	SD1 command
X2A17	X_SD1_CLK	O	VDD_SD1	SD1 clock
X2A19	reference-voltage	REF_O	VDD_SD1	SD1 reference voltage
X2A20	X_SD1_nWP	I	VDD_SD1	SD1 write protection (active low)
X2A21	X_SD1_nCD	I	VDD_SD1	SD1 card detection (active low)
X2A22	X_SD1_D0	I/O	VDD_SD1	SD1 data 0
X2A23	X_SD1_D1	I/O	VDD_SD1	SD1 data 1
X2A25	X_SD1_D2	I/O	VDD_SD1	SD1 data 2

Table 15: Location of SD/ MMC Card Interface Signals (continued)

8 Serial Interfaces

The phyFLEX-i.MX 6 provides numerous serial interfaces some of which are equipped with a transceiver to allow direct connection to external devices:

1. Two High speed UARTs (TTL, derived from UART3 and UART4 of the i.MX 6) with up to 4 MHz and one with hardware flow control (RTS and CTS signals)
2. High speed USB OTG interface (extended directly from the i.MX 6's USB-HS OTG PHY (USB-PHY))
3. High speed USB HOST interface (extended directly from the i.MX 6 USB HOST PHY (USB-PHY))
4. Auto-MDIX enabled 10/100/1000 Mbit Ethernet interface
5. Two I^2C interface (derived from I^2C port 2 and port 3 of the i.MX 6)
6. Two Serial Peripheral Interface (SPI) interface (extended from the third and fifth SPI module (eCSPI3 and eCSPI5) of the i.MX 6)
7. I^2S audio interface (originating from the fifth module of the i.MX 6's Synchronous Serial Interface (SSI5))
8. CAN 2.0B interface (extended directly from the i.MX 6 FlexCAN1 module)
9. SATA II, 3.0 Gbps (extended directly from the i.MX 6 SATA PHY)
10. PCI Express Gen. 2.0 (extended directly from the i.MX 6 PCIe PHY)
11. Media Local Bus (MLB) interface (connecting to the i.MX 6's MediaLB 150 block)

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

8.1 Universal Asynchronous Interface

The phyFLEX-i.MX 6 provides two high speed universal asynchronous interfaces with up to 4 MHz and one with additional hardware flow control (RTS and CTS signals). The following table shows the location of the signals on the phyFLEX-Connector.

Pin #	Signal	ST	Voltage Domain	Description
X1A12	X_UART1_TxD_TTL	O	VDD_3V3_LOGIC	UART3 serial transmit signal
X1A13	X_UART1_RxD_TTL	I	VDD_3V3_LOGIC	UART3 serial data receive signal
X1A14	X_UART1_RTS_TTL	O	VDD_3V3_LOGIC	UART3 request to send
X1A15	X_UART1_CTS_TTL	I	VDD_3V3_LOGIC	UART3 clear to send
X1A17	reference-voltage	REF_O	VDD_3V3_LOGIC	UART3 reference voltage
X1A18	X_UART0_TxD_TTL	O	VDD_3V3_LOGIC	UART4 serial transmit signal
X1A19	reference-voltage	REF_O	VDD_3V3_LOGIC	UART4 reference voltage
X1A20	X_UART0_RxD_TTL	I	VDD_3V3_LOGIC	UART4 serial data receive signal

Table 16: Location of the UART Signals

The signals extend from UART3 respectively UART4 of the i.MX 6 directly to the phyFLEX-Connector without conversion to RS-232 level. External RS-232 transceivers must be attached by the user if RS-232 levels are required.

8.2 USB OTG Interface

The phyFLEX-i.MX 6 provides a high speed USB OTG interface which uses the i.MX 6 embedded HS USB OTG PHY. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyFLEX-i.MX 6 USB OTG functionality. The applicable interface signals can be found on the phyFLEX-fix Connector X1 as shown in *Table 17*.

Pin #	Signal	ST	Voltage Domain	Description
X1A37	X_USB0_nVBUSEN	O	VDD_3V3_LOGIC	USB0 VBUS enable (active low)
X1A38	X_USB0_VBUS	PWR_I	5V	USB0 VBUS input
X1A39	X_USB0_nOC	IPU	VDD_3V3_LOGIC	USB0 overcurrent pin
X1A41	reference-voltage	REF_O	VDD_3V3_LOGIC	USB0 reference voltage
X1A42	X_USB0_CHGDET	O	VDD_3V3_LOGIC	USB0 charger detection
X1B38	X_USB0_D-	USB_I/O	i.MX 6 internal	USB0 data-
X1B39	X_USB0_D+	USB_I/O	i.MX 6 internal	USB0 data+
X1B40	X_USB0_ID	I	VDD_3V3_LOGIC	USB0 ID Pin

Table 17: Location of the USB OTG Signals

8.3 USB Host Interface

The phyFLEX-i.MX 6 provides a high speed USB Host interface which uses the i.MX 6 embedded HS USB Host PHY.

An external USB Standard-A (for USB host) connector is all that is needed to interface the phyFLEX-i.MX 6 USB Host functionality. The applicable interface signals (D+/D-/ PWR/OC) can be found on the phyFLEX-fix Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1A43	X_USB1_nVBUSEN	O	VDD_3V3_LOGIC	USB1 VBUS enable (active low)
X1A44	X_USB1_VBUS	PWR_I	5V	USB1 VBUS input
X1A45	X_USB1_nOC	IPU	VDD_3V3_LOGIC	USB1 overcurrent pin
X1A47	reference-voltage	REF_O	VDD_3V3_LOGIC	USB1 reference voltage
X1B44	X_USB1_D-	USB_I/O	i.MX 6 internal	USB0 data-
X1B45	X_USB1_D+	USB_I/O	i.MX 6 internal	USB0 data+

Table 18: Location of the USB-Host Signals

8.4 Ethernet Interface

Connection of the phyFLEX-i.MX 6 to the world wide web or a local area network (LAN) is possible using the on-board GbE PHY at U11. It is connected to the RGMII interface of the i.MX 6. The PHY operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s or 1000 Mbit/s.

8.4.1 Ethernet PHY (U11)

With an Ethernet PHY mounted at U11 the phyFLEX-i.MX 6 has been designed for use in 10Base-T, 100Base-T and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyFLEX-fix Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1B24	X_ETH0_ANALOG_ VOLTAGE	REF_O	VDD_3V3_LOGIC	ETH0 reference voltage for 10/100Mbit , for phyFLEX-i.MX 6 this pin is only connected to a 100 nF capacitor tied to ground
X1B26	X_ETH0_A+/TX0+	ETH_O	VDD_3V3_LOGIC	ETH0 data A+ /transmit+
X1B27	X_ETH0_A-/TX0-	ETH_O	VDD_3V3_LOGIC	ETH0 data A-/transmit-
X1B28	X_ETH0_LED0	OC	VDD_3V3_LOGIC	ETH0 link LED output
X1B29	X_ETH0_B+/RX0+	ETH_I	VDD_3V3_LOGIC	ETH0 data B+/receive+
X1B30	X_ETH0_B-/RX0-	ETH_I	VDD_3V3_LOGIC	ETH0 data B-/receive-
X1B32	X_ETH0_C+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C+ (only GbE)
X1B33	X_ETH0_C-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C- (only GbE)
X1B34	X_ETH0_LED1	OC	VDD_3V3_LOGIC	ETH0 traffic LED output
X1B35	X_ETH0_D+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D+ (only GbE)
X1B36	X_ETH0_D-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D- (only GbE)

Table 19: Location of the Ethernet Signals

The on board GbE PHY supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX

pins accordingly. The Ethernet PHY also features an Auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet controller is connected to the RGMII interface of the i.MX 6. Please refer to the *i.MX 6 Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network some external circuitry is required. The required termination resistors on the analog signals (ETH0_A±, ETH0_B±, ETH0_C±, ETH0_D±) are integrated in the chip, so there is no need to connect external termination resistors to these signals. Connection to an external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+,C- and D+/D- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

If you are using the applicable carrier board for the phyFLEX-i.MX 6 (part number PBA-B-01), the external circuitry mentioned above is already integrated on the board (refer to *section* ***Error! Reference source not found.***).

Caution!
Please see the datasheet of the Ethernet PHY when designing the Ethernet transformer circuitry.

8.4.2 Software Reset of the Ethernet Controller

The Ethernet PHY at U11 can be reset by software. The reset input of the Ethernet PHY is permanently connected to Pad EIM_D23 (GPIO3_23) of the i.MX 6.

8.4.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyFLEX-i.MX 6 is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

8.5 I²C Interface

The Inter-Integrated Circuit (I²C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 6 contains three identical and independent multimaster fast-mode I²C modules. The interface of the second and third module (I2C2 and I2C3) are available on the phyFLEX-Connectors. The first module connects to the on-board EEPROM (refer to *section 6.3)* and to the EMIC at U19 (see *section 15*). Both I2C interfaces which are brought out on the connector have on board resistors which are laid-out for a capacitive load of max. 150 pF in fast mode. The following table lists the I²C port on the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X1A68	X_I2C0_SDA	I/O	VDD_3V3_LOGIC	I2C0 data
X1A69	X_I2C0_SCL	I/O	VDD_3V3_LOGIC	I2C0 clock
X1A71	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C0 reference voltage
X2A1	X_I2C1_SDA	I/O	VDD_3V3_LOGIC	I2C1 data
X2A2	X_I2C1_SCL	I/O	VDD_3V3_LOGIC	I2C1 clock
X2A3	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C1 reference voltage

Table 20: I²C Interface Signal Location

8.6 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyFLEX provides two SPI interfaced on the phyFLEX-fix connector X1. The SPI interfaces provide three respectively two chip select signals. The Enhanced Configurable SPI (ECSPI) of the i.MX 6 has five separate modules (ECSPI1, ECSPI2, ECSPI3, ECSPI4 and ECSPI5) which support data rates of up to 20 Mbit/s. The interface signals of the third and fifth module (ECSPI3, ECSPI5) are made available on the phyFLEX-Connector. This module is master/slave configurable. The following table lists the SPI signals on the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X1A21	X_SPI0_MOSI	O	VDD_3V3_LOGIC	SPI0 master output/slave input
X1A23	X_SPI0_MISO	I	VDD_3V3_LOGIC	SPI0 master input/slave output
X1A24	X_SPI0_CSBOOT	O	VDD_3V3_LOGIC	SPI0 chip select BOOT
X1A25	X_SPI0_CS0	O	VDD_3V3_LOGIC	SPI0 chip select 0
X1A26	X_SPI0_CS1	O	VDD_3V3_LOGIC	SPI0 chip select 1
X1A27	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI0 reference voltage
X1A29	X_SPI0_CLK	O	VDD_3V3_LOGIC	SPI0 clock signal
X1A30	X_SPI1_CS0	O	VDD_3V3_LOGIC	SPI1 chip select 0
X1A31	X_SPI1_MOSI	O	VDD_3V3_LOGIC	SPI1 master output/slave input
X1A32	X_SPI1_MISO	I	VDD_3V3_LOGIC	SPI1 master input/slave output
X1A33	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI1 reference voltage
X1A35	X_SPI1_CLK	O	VDD_3V3_LOGIC	SPI1 clock signal
X1A36	X_SPI1_CS1	O	VDD_3V3_LOGIC	SPI1 chip select 1

Table 21: SPI Interface Signal Location

8.7 I²S Audio Interface (SSI))

The Synchronous Serial Interface (SSI) of the phyFLEX-i.MX 6 is a full-duplex, serial interface that allows to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I^2S) and Intel AC'97 standard. The i.MX 6 provides three instances of the SSI module. On the phyFLEX-i.MX 6 SSI5 is brought out to the phyFLEX-Connector.

With reference to the phyFLEX specification, the main purpose of this interface is to connect to an external codec, such as I^2S. Four signals extend from the i.MX 6 SSI module to the phyFLEX-Connector (I2S0_CLK, I2S0_FRM, I2S0_ADC, I2S0_DAC).

Pin #	Signal	ST	Voltage Domain	Description
X1A48	X_I2S0_CLK	I/O	VDD_3V3_LOGIC	I^2S clock
X1A49	X_I2S0_FRM	I/O	VDD_3V3_LOGIC	I^2S frame
X1A50	X_I2S0_ADC	I	VDD_3V3_LOGIC	I^2S receive data
X1A51	reference-voltage	REF_O	VDD_3V3_LOGIC	I^2S reference voltage
X1A53	X_I2S0_DAC	O	VDD_3V3_LOGIC	I^2S transmit data

Table 22: I^2S Interface Signal Location

8.8 CAN Interface

The CAN interface of the phyFLEX-i.MX 6 is connected to the first FlexCAN module (FlexCAN1) of the i.MX 6 which is a full implementation of the CAN protocol specification Version 2.0B. It supports standard and extended message frames and programmable bit rates of up to 1 Mb/s.
The signals of the CAN interface are brought out on the phyFLEX-optional connector X2. The following table shows the position of the signals.

Pin #	Signal	ST	Voltage Domain	Description
X2A4	X_CAN0_TXD	O	VDD_3V3_LOGIC	CAN0 transmit
X2A5	X_CAN0_RXD	I	VDD_3V3_LOGIC	CAN0 receive
X2A7	reference-voltage	REF	VDD_3V3_LOGIC	CAN0 reference voltage

Table 23: CAN Interface Signal Location

8.9 SATA Interface

The SATA II interface of the phyFLEX-i.MX 6 is a high-speed serialized ATA data link interface compliant with SATA Revision 3.0 (physical layer complies with SATA Revision 2.5) which supports data rates of up to 3.0 Gbit/s. The interface includes an internal DMA engine, command layer, transport layer, link layer and the physical layer. The interface itself supports only one SATA device.

The phyFLEX-i.MX 6 provides an SATA II Interface at the phyFLEX-optional connector X2 at the following locations:

Pin #	Signal	ST	Voltage Domain	Description
X2A10	X_SATA0_TX+	LVDS_O	i.MX 6 internal	SATA0 transmit lane+
X2A11	X_SATA0_TX-	LVDS_O	i.MX 6 internal	SATA0 transmit lane-
X2A13	X_SATA0_RX+	LVDS_I	i.MX 6 internal	SATA0 receive lane+
X2A14	X_SATA0_RX-	LVDS_I	i.MX 6 internal	SATA0 receive lane-

Table 24: SATA Interface Signal Location

8.10 PCI Express Interface

The 1-lane PCI Express interface of the phyFLEX-i.MX 6 provides PCIe Gen. 2.0 functionality which supports 5 Gbit/s operation. Furthermore the interface is fully backwards compatible to the 2.5 Gbit/s Gen. 1.1 specification. The present and the wake signals are realized by GPIOs.

Table 25 shows the position of the PCIe signals on the phyFLEX-fix connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1B65	X_PCIe0_nPRSNT	I/O	VDD_3V3_LOGIC	PCIe0 present signal (low active)
X1B66	reference-voltage	REF_O	VDD_3V3_LOGIC	PCIe0 reference voltage
X1B68	X_PCIe0_TX+	PCIe_O	i.MX 6 internal	PCIe0 transmit lane+
X1B69	X_PCIe0_TX-	PCIe_O	i.MX 6 internal	PCIe0 transmit lane-
X1B70	X_PCIe0_nWAKE	I/O	VDD_3V3_LOGIC	PCIe0 wake signal (low active)
X1B71	X_PCIe0_RX+	PCIe_I	i.MX 6 internal	PCIe0 receive lane+
X1B72	X_PCIe0_RX-	PCIe_I	i.MX 6 internal	PCIe0 receive lane-
X1B74	X_PCIe0_CLK+	PCIe_O	i.MX 6 internal	PCIe0 clock lane+
X1B75	X_PCIe0_CLK-	PCIe_O	i.MX 6 internal	PCIe0 clock lane-

Table 25: PCIe Interface Signal Location

8.11 Media Local Bus

The Media Local Bus (MLB) interface provides a link to a MOST® data network, using the standardized Media Local Bus protocol (up to 150 Mbit/s) for inter-chip communication. The Media Local Bus interface is implemented as MediaLB 6-pin interface (differential). The module is backward compatible to MLB-50. The MLB interface is only available on the not standardized phyFLEX-flex connector X3. The following table shows the position of the signals on the connector.

Pin #	Signal	ST	Voltage Domain	Description
X3B16	X_MLB_DP	MLB_I/O	i.MX 6 internal	Media local bus data line+
X3B17	X_MLB_DN	MLB_I/O	i.MX 6 internal	Media local bus data line-
X3B19	X_MLB_SP	MLB_I/O	i.MX 6 internal	Media local bus signal line+
X3B20	X_MLB_SN	MLB_I/O	i.MX 6 internal	Media local bus signal line-
X3B22	X_MLB_CP	MLB_O	i.MX 6 internal	Media local bus clock+
X3B23	X_MLB_CN	MLB_O	i.MX 6 internal	Media local bus clock-

Table 26: Media Local Bus Interface Signal Location

9 General Purpose I/Os

The phyFLEX bus provides 11 GPIO signals. *Table 27* shows the location of the GPIO pins on the phyFLEX-Connector, as well as the corresponding ports of the i.MX 6.

Pin #	Signal	ST	Voltage Domain	Description
X1A54	X_GPIO0	I/O	VDD_3V3_LOGIC	General purpose input/output 0 (GPIO5_8 of i.MX 6)
X1A55	X_GPIO1	I/O	VDD_3V3_LOGIC	General purpose input/output 1 (GPIO5_7 of i.MX 6)
X1A56	X_GPIO2	I/O	VDD_3V3_LOGIC	General purpose input/output 2 (GPIO4_18 of i.MX 6)
X1A57	reference-voltage	REF_O	VDD_3V3_LOGIC	GPIO reference voltage
X1A59	X_GPIO3	I/O	VDD_3V3_LOGIC	General purpose input/output 3 (GPIO4_19 of i.MX 6)
X1A60	X_GPIO4	I/O	VDD_3V3_LOGIC	General purpose input/output 4 (GPIO1_6 of i.MX 6)
X1A61	X_GPIO5	I/O	VDD_3V3_LOGIC	General purpose input/output 5 (GPIO1_9 of i.MX 6)
X1A62	X_GPIO6	I/O	VDD_3V3_LOGIC	General purpose input/output 6 (GPIO7_12 of i.MX 6)

Table 27: Location of GPIO Pins

Pin #	Signal	ST	Voltage Domain	Description
X1A63	X_GPIO7	I/O	VDD_3V3_LOGIC	General purpose input/output 7 (GPIO7_13 of i.MX 6)
X1A65	X_GPIO8	I/O	VDD_3V3_LOGIC	General purpose input/output 8 (GPIO4_5 of i.MX 6)
X1A66	X_GPIO9	I/O	VDD_3V3_LOGIC	General purpose input/output 9 (GPIO2_23 of i.MX 6)
X1A67	X_GPIO10	I/O	VDD_3V3_LOGIC	General purpose input/output 10 (GPIO2_24 of i.MX 6)

Table 27: Location of GPIO Pins (continued)

Beside these 11 dedicated GPIOs, most of the i.MX 6 signals which are connected directly to the module connector can be configured to act as GPIOs, due to the multiplexing functionality of most controller pins.

10 User LEDs

The phyFLEX-i.MX 6 provides two user LEDs on board, a red (D2) and a green (D1). D2 can be controlled by setting GPIO2_31 (pad EIM_EB3) and D1 can by controlled by setting GPIO1_30 (pad ENET_TXD0) to the desired output level. A high-level turns the LED on, a low-level turns it off.

11 Debug Interface (X1, X4)

The phyFLEX-i.MX 6 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends to the phyFLEX-fix connector X1 and also to a 2.0 mm pitch pin header at X4 on the edge of the module PCB.

Table 28 shows the location of the JTAG pins on the phyFLEX-fix connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1A5	X_JTAG_nTRST	I	VDD_3V3_LOGIC	JTAG reset input
X1A6	X_JTAG_TDI	I	VDD_3V3_LOGIC	JTAG TDI
X1A7	X_JTAG_TMS	I	VDD_3V3_LOGIC	JTAG TMS
X1A8	X_JTAG_TDO	O	VDD_3V3_LOGIC	JTAG TDO
X1A9	X_JTAG_TCK	I	VDD_3V3_LOGIC	JTAG clock input
X1A10	GND	-	-	Ground 0 V
X1A11	X_JTAG_RTCLK	O	VDD_3V3_LOGIC	JTAG RTCLK
X1B5	reference-voltage	REF_O	VDD_3V3_LOGIC	JTAG reference voltage

Table 28: Debug Interface Signal Location at phyFLEX-Connector X1

Figure 9 and *Figure 10* show the position of the debug interface (JTAG connector X4) on the phyFLEX-i.MX 6 module.

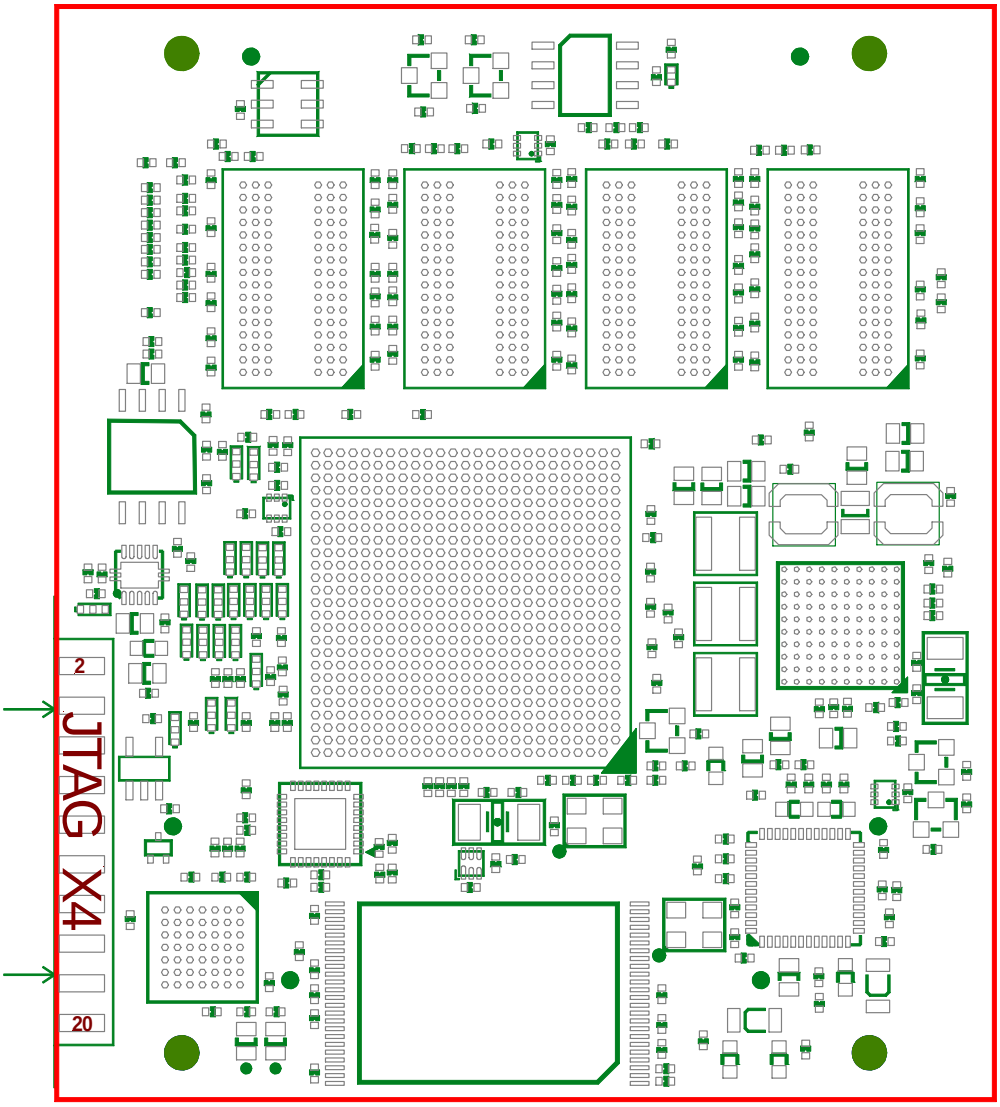

Figure 9: JTAG Interface at X4 (top view)

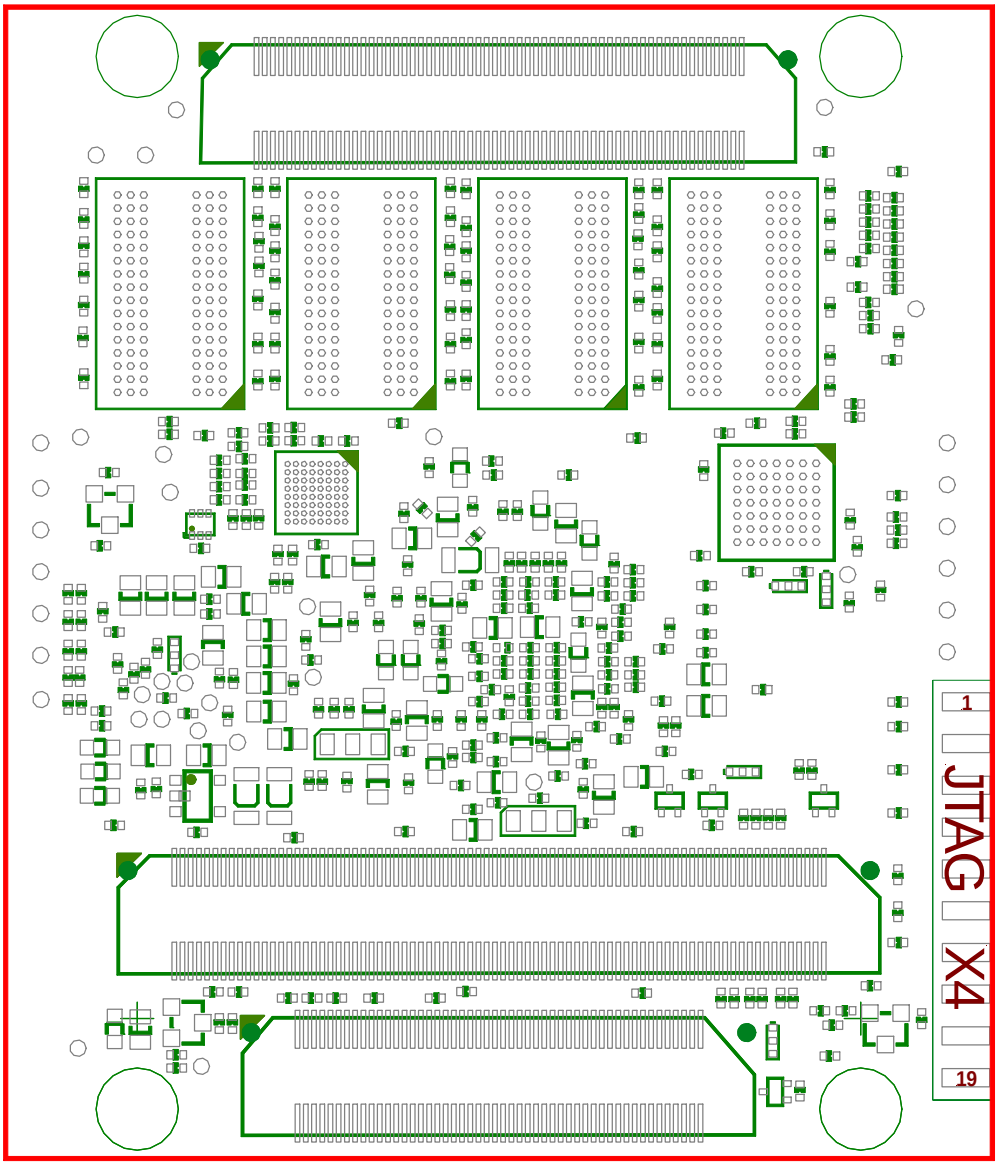

Figure 10: JTAG Interface at X4 (bottom view)

Pin 1 of the JTAG connector X4 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Table 29 shows details on the JTAG signal pin assignment.

Note:
The JTAG connector X4 only populates phyFLEX-i.MX 6 modules with a specific order option. We recommend integration of a standard (2 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface.

Signal	Pin Row*		Signal
	A	B	
VSUPPLY (VDD_3V3_LOGIC)	2	1	TREF (VDD_3V3_LOGIC via 0 Ohms)
GND	4	3	X_JTAG_TRSTB
GND	6	5	X_JTAG_TDI
GND	8	7	X_JTAG_TMS
GND	10	9	X_JTAG_TCK
GND	12	11	X_JTAG_RTCK (connected via 0 Ohms to X_JTAG_TCK)
GND	14	13	X_JTAG_TDO
GND	16	15	X_PM_nRESET_IN
GND	18	17	not connected
GND	20	19	not connected

Table 29: JTAG Connector X4 Signal Assignment

***Note:** Row A is on the controller side of the module and row B is on the connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyFLEX-i.MX 6 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X4 to standard Emulator connectors.

12 LVDS Display Interface

The LVDS-Signals from the on-chip LVDS Display Bridge (LDB) of the i.MX 6 are brought out at the phyFLEX-fix connector X1. Thus an LVDS-Display can connect directly to the phyFLEX-i.MX 6. The location of the applicable interface signals (X_LVDS0_L0-3+, X_LVDS0_L0-3-, X_LVDS0_CLK+ and X_LVDS0_CLK-) and of the two control signals display enable and backlight PWM (nLVDS0_DISP_EN and LVDS0_DISP_BL_PWM) can be found in the table below.

Pin #	Signal	ST	Voltage Domain	Description
X1B50	X_LVDS0_L0+	LVDS_O	i.MX 6 internal	LVDS0 data0+
X1B51	X_LVDS0_L0-	LVDS_O	i.MX 6 internal	LVDS0 data0-
X1B52	X_LVDS0_nDISP_EN	O	VDD_3V3_LOGIC	LVDS0 display enable (low active)
X1B53	X_LVDS0_L1+	LVDS_O	i.MX 6 internal	LVDS0 data1+
X1B54	X_LVDS0_L1-	LVDS_O	i.MX 6 internal	LVDS0 data1-
X1B56	X_LVDS0_L2+	LVDS_O	i.MX 6 internal	LVDS0 data2+
X1B57	X_LVDS0_L2-	LVDS_O	i.MX 6 internal	LVDS0 data2-
X1B58	X_LVDS0_DISP_BL_PWM	O	VDD_3V3_LOGIC	LVDS0 backlight PWM output
X1B59	X_LVDS0_L3+	LVDS_O	i.MX 6 internal	LVDS0 data3+
X1B60	X_LVDS0_L3-	LVDS_O	i.MX 6 internal	LVDS0 data3-
X1B62	X_LVDS0_CLK+	LVDS_O	i.MX 6 internal	LVDS0 clock+
X1B63	X_LVDS0_CLK-	LVDS_O	i.MX 6 internal	LVDS0 clock-
X1B64	reference-voltage	REF_O	VDD_3V3_LOGIC	LVDS0 reference voltage

Table 30: Display Interface Signal Location

Furthermore the phyFLEX-i.MX 6 supports a second LVDS Display at the non standardized phyFLEX-flex connector X3. The table below shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X3B1	X_LVDS1_TX0_P	LVDS_O	i.MX 6 internal	LVDS1 data0+
X3B2	X_LVDS1_TX0_N	LVDS_O	i.MX 6 internal	LVDS1 data0-
X3B4	X_LVDS1_TX1_P	LVDS_O	i.MX 6 internal	LVDS1 data1+
X3B5	X_LVDS1_TX1_N	LVDS_O	i.MX 6 internal	LVDS1 data1-
X3B7	X_LVDS1_TX2_P	LVDS_O	i.MX 6 internal	LVDS1 data2+
X3B8	X_LVDS1_TX2_N	LVDS_O	i.MX 6 internal	LVDS1 data2-
X3B10	X_LVDS1_TX3_P	LVDS_O	i.MX 6 internal	LVDS1 data3+
X3B11	X_LVDS1_TX3_N	LVDS_O	i.MX 6 internal	LVDS1 data3-
X3B13	X_LVDS1_CLK_P	LVDS_O	i.MX 6 internal	LVDS1 clock+
X3B14	X_LVDS1_CLK_N	LVDS_O	i.MX 6 internal	LVDS1 clock-

Table 31: Second Display Interface Signal Location at X3

12.1 LVDS Display Interface pixel mapping

The phyFLEX specification defines the pixel mapping of the LVDS display interface. The pixel mapping equates to the OpenLDI respectively Intel 24.0 or JEIDA standard. Thus you can connect 18-bit as well as 24-bit LVDS displays to the phyFLEX. *Table 32* and *Table 33* show the recommended pixel mapping of the LVDS display. However since the i.MX 6 LDB Module supports also the SPWG pixel mapping, this one can be used as well by setting the appropriated configuration bit.

Note:
To be fully compatible to the phyFLEX specification, make sure that the LVDS display you want to use provides the same pin mapping as the phyFLEX (JEIDA respectively OpenLDI). Normally this is only important for 24-bit LVDS displays because due to the organization of the LVDS pixel mapping all common 18-bit LVDS displays should work.

18-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G0	R5	R4	R3	R2	R1	R0
A1	B1	B0	G5	G4	G3	G2	G1
A2	DE	VSYNC	HSYNC	B5	B4	B3	B2
A3	0	0	0	0	0	0	0

Table 32: Pixel Mapping of 18-bit LVDS Display Interface

24-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G2	R7	R6	R5	R4	R3	R2
A1	B3	B2	G7	G6	G5	G4	G3
A2	DE	VSYNC	HSYNC	B7	B6	B5	B4
A3	0	B1	B0	G1	G0	R1	R0

Table 33: Pixel Mapping of 24-bit LVDS Display Interface

13 High-Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface (HDMI) of the phyFLEX-i.MX 6 is compliant to HDMI 1.4 and DVI 1.0. It supports a maximum pixel clock of up to 340 MHz for up to 720p at 100 Hz and 720i at 200 Hz, or 1080p at 60 Hz and 1080i/720i at 120 Hz HDTV display resolutions, and a graphic display resolution of up to 2048x1536 (QXGA). Please refer to the *i.MX 6 Reference Manual* for more information.

The following table shows the location of the HDMI signals on the phyFLEX-optional connector X2.

Pin #	Signal	ST	Voltage Domain	Description
X2A8	X_HDMI0_SDA	I/O	VDD_3V3_LOGIC	HDMI0 I2C data
X2A9	X_HDMI0_SCL	I/O	VDD_3V3_LOGIC	HDMI0 I2C clock
X2B1	X_HDMI0_TMDS_DATA2+	TMDS_O	i.MX 6 internal	HDMI0 data2+
X2B2	X_HDMI0_TMDS_DATA2-	TMDS_O	i.MX 6 internal	HDMI0 data2-
X2B4	X_HDMI0_TMDS_DATA1+	TMDS_O	i.MX 6 internal	HDMI0 data1+
X2B5	X_HDMI0_TMDS_DATA1-	TMDS_O	i.MX 6 internal	HDMI0 data1-
X2B6	reference-voltage	REF_O	VDD_3V3_LOGIC	HDMI0 reference voltage
X2B7	X_HDMI0_TMDS_DATA0+	TMDS_O	i.MX 6 internal	HDMI0 data0+
X2B8	X_HDMI0_TMDS_DATA0-	TMDS_O	i.MX 6 internal	HDMI0 data0-
X2B10	X_HDMI0_TMDS_CLOCK+	TMDS_O	i.MX 6 internal	HDMI0 clock+
X2B11	X_HDMI0_TMDS_CLOCK-	TMDS_O	i.MX 6 internal	HDMI0 clock-
X2B12	X_HDMI0_CEC	I/O	VDD_3V3_LOGIC	HDMI0 CEC
X2B13	X_HDMI0_nHPD	I	VDD_3V3_LOGIC	HDMI0 hot plug detect

Table 34: HDMI Interface Signal Location at X2

14 LVDS Camera Interface

The phyFLEX-i.MX 6 uses two 1-channel 10-Bit LVDS Random Lock Deserializer (U12 and U27) to receive LVDS-Signals from a LVDS Camera Interface. The LVDS Deserializer converts the LVDS Signals to a 10-bit wide parallel data bus and separate clock which can be used as inputs for the i.MX 6 Camera Sensor Interfaces (U12 is connected to CSI1 and U27 is connected to CSI0). The 10-bit wide data bus consists of 8 color information bits and 2 sync bits (HSYNC/VSYNC).

The following table shows the location of the applicable interface signals (X_CAMERAx_CLK, X_CAMERAx_L+, X_CAMERAx_L-) on the phyFLEX-Connector.

Pin #	Signal	ST	Voltage Domain	Description
X2A40	X_CAMERA0_L0+	LVDS_I	VDD_3V3_LOGIC	Camera0 data+
X2A41	X_CAMERA0_L0-	LVDS_I	VDD_3V3_LOGIC	Camera0 data-
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera0 master clock
X2A44	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera0 reference voltage
X2A46	X_CAMERA1_L0+	LVDS_I	VDD_3V3_LOGIC	Camera1 data+
X2A47	X_CAMERA1_L0-	LVDS_I	VDD_3V3_LOGIC	Camera1 data-
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera1 master clock
X2A50	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera1 reference voltage

Table 35: Camera Interface Signal Location at X2

To assists the implementation of a power management the Deserializer's REN inputs are connected to the CSI0_DATA_EN pad (U27) respectively to the EIM_DA10 pad (U12) of the i.MX 6. Furthermore the nPWRDN signals of the Deserializers are connected to the ENET_RX_ER pad (U27) respectively to the EIM_EB0 pad (U12) of the i.MX 6. Thereby the LVDS Deserializer can be turned off by software.

14.1 Signal Configuration (J9 and J31)

J9 selects rising, or falling edge strobe for the LVDS Deserializer at U12 used for the camera connectivity of the phyFLEX-i.MX 6 CSI1 port.

J31 selects rising, or falling edge strobe for the LVDS Deserializer at U27 used for the camera connectivity of the phyFLEX-i.MX 6 CSI0 port.

Position	Description	Type
2+3	**rising edge strobe used for the LVDS camera signals**	0R (0402)
1+2	falling edge strobe used for the LVDS camera signals	

Table 36: LVDS Signal Configuration J9 and J31

15 Environment Management IC (EMIC) (U19)

The optional Environment Management IC (EMIC) at U19 gives the possibility to detect, monitor and record particular physical parameter such as current consumption, temperature und voltages. Furthermore the Environment Management IC comes with a PWM output and a tacho input for fan controlling and an I^2C Management bus.

16 Technical Specifications

The physical dimensions of the phyFLEX-i.MX 6 are represented in *Figure 11*. The module's profile is max. 10 mm thick, with a maximum component height of 3.0 mm on the bottom (connector) side of the PCB and approximately 5.0 mm on the top (microcontroller) side. The board itself is approximately 1.4 mm thick.

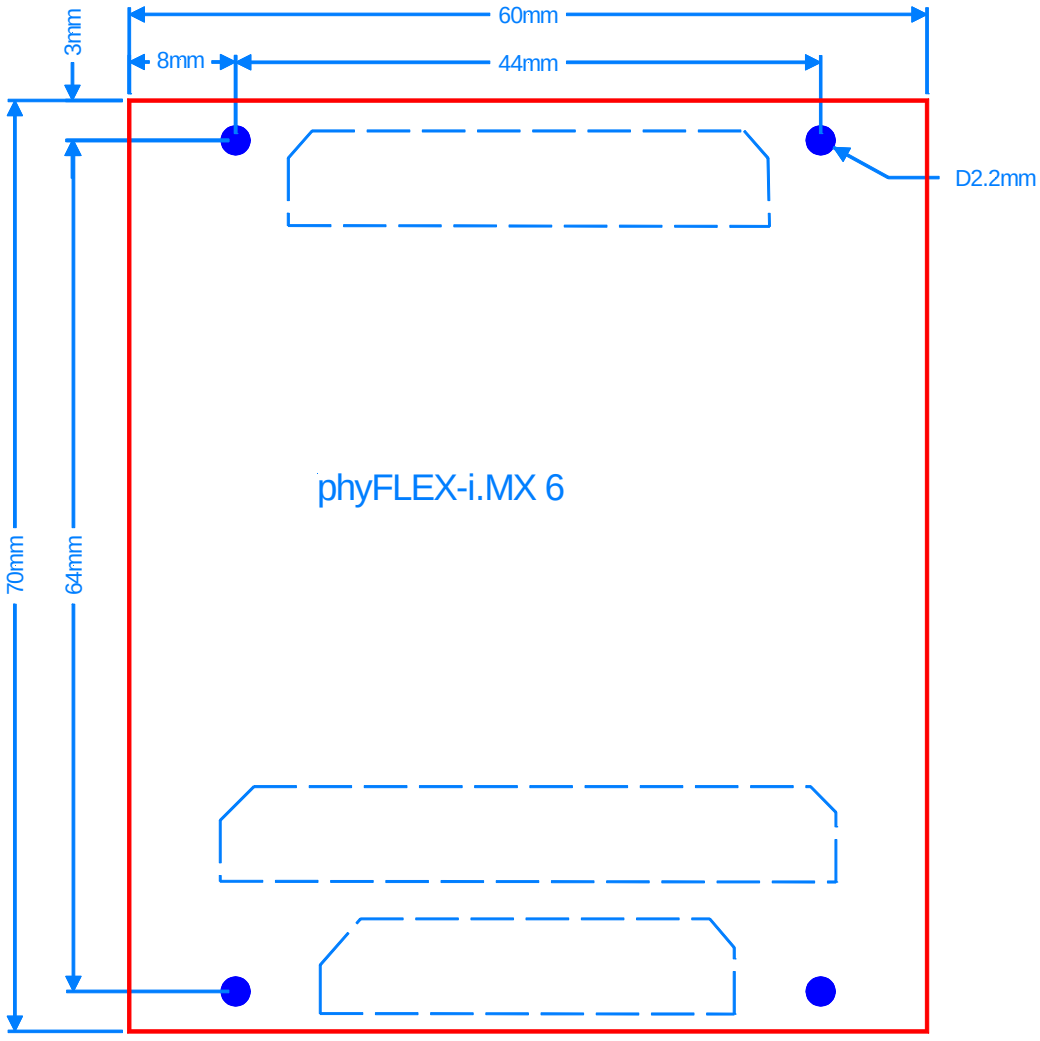

Figure 11: Physical Dimensions (top view)

Note:
To facilitate the integration of the phyFLEX-i.MX 6 into your design, the footprint of the phyFLEX-i.MX 6 is available for download (see *section 17.1*).

Additional specifications:

Dimensions:	60 mm x 70 mm
Weight:	TBD
Storage temperature:	-40°C to +125°C
Operating temperature:	0°C to +70°C (commercial) -40°C to +85°C (industrial)
Humidity:	95% r.F. not condensed
Operating voltage:	VCC 5 V +/- 5%
Power consumption:	TBD

These specifications describe the standard configuration of the phyFLEX-i.MX 6 as of the printing of this manual.

Connectors on the phyFLEX-i.MX 6:

Manufacturer	Samtec
	phyFLEX-fix (X1):
Number of pins per contact rows	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	BSH-080-01-L-D-A-K-TR
	phyFLEX-optional (X2):
Number of pins per contact rows	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	BSH-050-01-L-D-A-K-TR
	phyFLEX-flex (X3):
Number of pins per contact rows	120 pins (2 rows of 60 pins each)
Samtec part number (lead free)	BSH-060-01-L-D-A

The following list shows the receptacle sockets that correspond to the connectors populating the underside of the phyFLEX—i.MX 6. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the bottom side of the phyFLEX must be subtracted.

Connector height 5 mm

Manufacturer	Samtec
Number of pins per contact row	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	ASP-167037-01 (BTH-080-01-L-D-A-K-TR)
PHYTEC part number (lead free)	VM245
Number of pins per contact row	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	BTH-050-01-L-D-A-K-TR
PHYTEC part number (lead free)	VM247
Number of pins per contact row	120 pins (2 rows of 60 pins each)
Samtec part number (lead free)	BTH-060-01-L-D-A
PHYTEC part number (lead free)	VM240

Please refer to the corresponding data sheets and mechanical specifications provided by Samtec (*www.samtec.com*).

17 Hints for Integrating and Handling the phyFLEX-i.MX 6

17.1 Integrating the phyFLEX-i.MX 6

Besides this hardware manual much information is available to facilitate the integration of the phyFLEX-i.MX 6 into customer applications.

1. the design of the standard phyFLEX Carrier Board can be used as a reference for any customer application
2. many answers to common questions can be found at http://www.phytec.de/de/support/faq/faq-phyFLEX-i.MX 6.html, or http://www.phytec.eu/europe/support/faq/faq-phyFLEX-i.MX 6.html
3. the link "Carrier Board" within the category Dimensional Drawing leads to the layout data as shown in *Figure 12*. It is available in different file formats. Use of this data allows to integrate the phyFLEX-i.MX 6 SOM as a single component into your design.
4. different support packages are available to support you in all stages of your embedded development. Please visit http://www.phytec.de/de/support/support-pakete.html, or http://www.phytec.eu/europe/support/support-packages.html, or contact our sales team for more details.

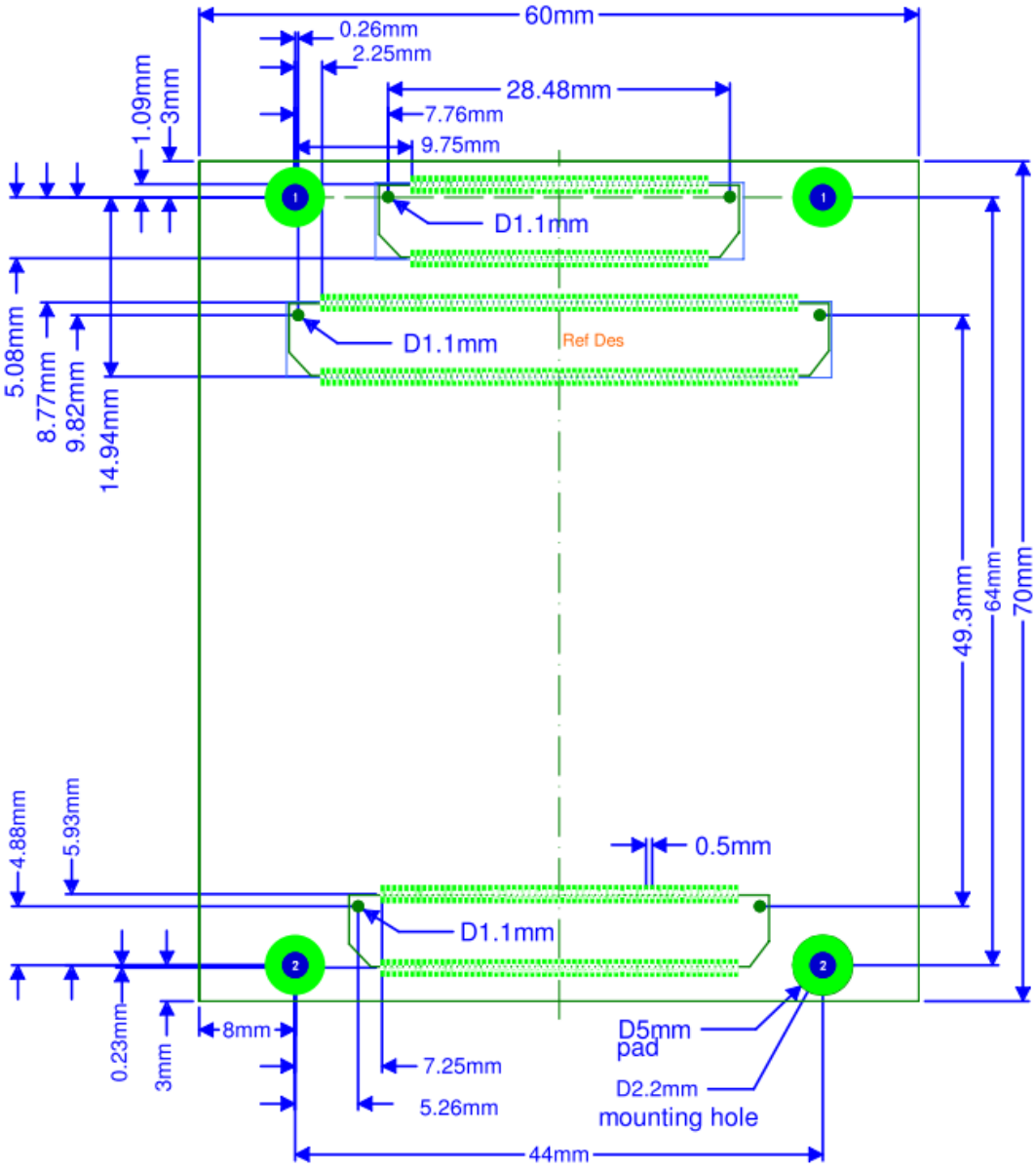

Figure 12: Footprint of the phyFLEX-i.MX 6

17.2 Handling the phyFLEX-i.MX 6

- **Modifications on the phyFLEX Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyFLEX into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyFLEX module. For maximum EMI performance we recommend as a general design rule to connect all GND pins to a solid ground plane. But at least all GND pins neighboring signals which are being used in the application circuitry should be connected to GND.

Published by PHYTEC

Ordering No. L-773e_2
Printed in Germany